

# Compal Confidential

## *Diner Braswell M/B LA-D704P Schematics Document*

**Intel Braswell + ATI R16M-M1-30/70**

**2015/12/12**

**Project Code : BDL50**

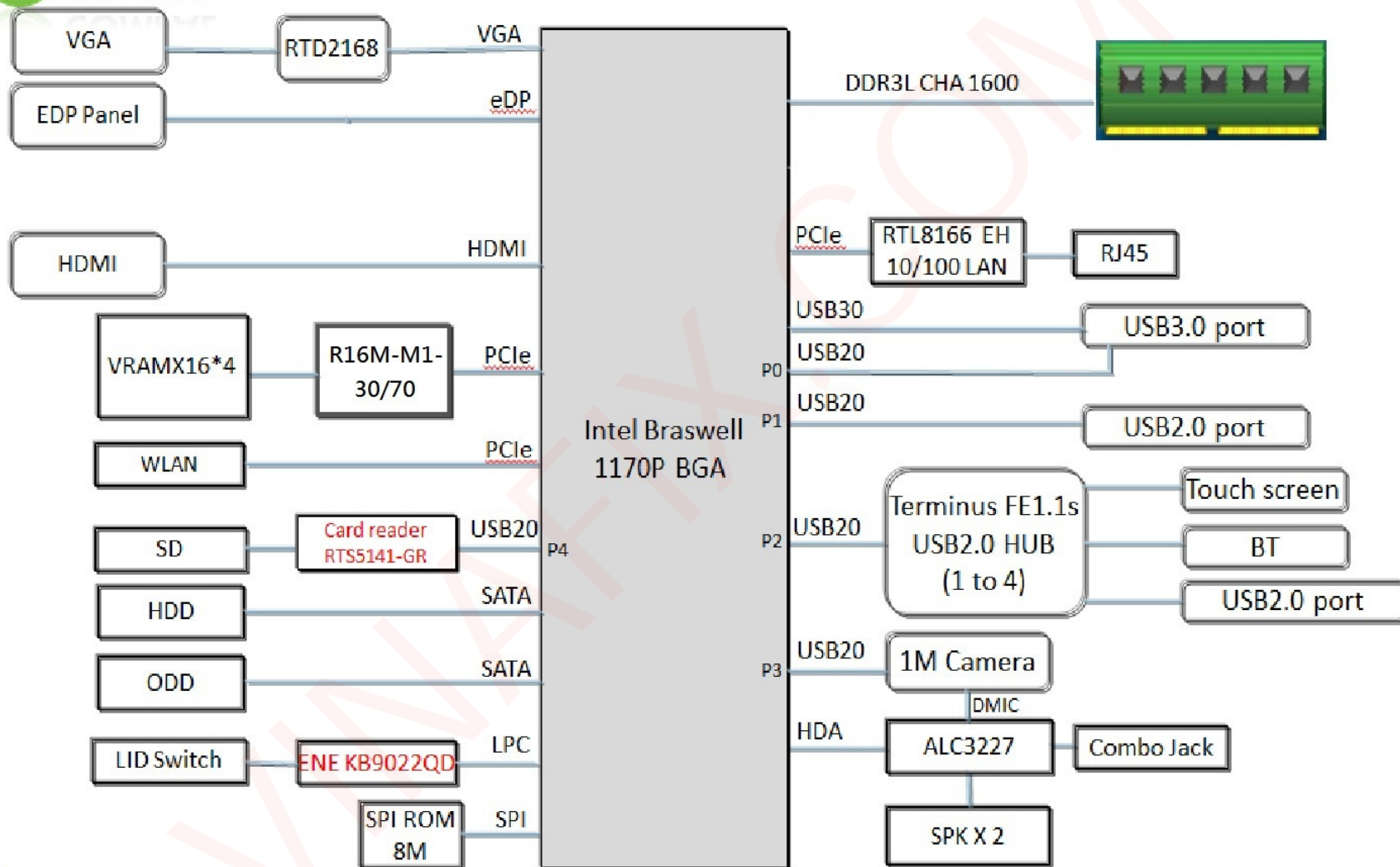
**Rev. 0.3 PV**

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# Intel Braswell 15"

# Hardware Block Diagram



## Sub-board

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CR+USB/B

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PWR BTN/B

page36

TP BTN/B

page24

HDD or SSD/B

page24

ODD/B

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## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

## <PCI-E,SATA,USB3.0>

Lane#	USB3.0	DESTINATION	
		UMA	DIS
0		USB3.0	USB3.0
1			

Lane#	SATA	DESTINATION	
		UMA	DIS
0		HDD	HDD
1		ODD	ODD

Lane#	PCIE	DESTINATION	
		UMA	DIS
0			GPU
1			GPU
2		WLAN	WLAN
3		LAN	LAN

## <USB2.0 port>

USB2.0 port	UMA	Dis
0	USB 3.0 (MB)	USB 3.0 (MB)
1	USB 2.0 (MB)	USB 2.0 (MB)
2	Camera	Camera
3	Card Reader	Card Reader
4	USB 2.0 Hub	USB 2.0 Hub

## <USB2.0 Hub>

USB2.0 port	UMA	Dis
0	Touch Screen	Touch Screen
1	USB 2.0 (SB)	USB 2.0 (SB)
2	BT	BT
3		
4		

## EC SM Bus1 address

Device	Address
Charger	
Battery	

## EC SM Bus2 address

CPU Thermal Sensor	4C	UC3
ATI GPU EXO Pro		U666

## EC SM Bus3 address

GPU Thermal Sensor	4C	UV1
--------------------	----	-----

## SOC SM Bus address

Device	Address
ChannelA	A0 DDR DIMM1
ChannelB	A2 DDR DIMM2
Touch Pad	

## BOM Structure Table

BOM Config	Description
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
PX@	For Discrete Sku
8166@	10/100 LAN
8151@	Giga LAN
UMA@	For UMA Sku
NAT@	EC Non Auto Load Code
AUTO@	EC Auto Load Code
TPM@	CPU to EC LPC use 3.3V level
NTPM@	CPU to EC LPC use 1.8V level
GCLK@	Pop Green Clock
GCUMA@	Pop Green Clock UMA
GCDIS@	Pop Green Clock DIS
XTAL@	For XTAL
TS@	Pop Touch Screen component
R30@	For R16M-M1-30 GPU
R70@	For R16M-M1-70 GPU
6U@	For 6U@ (Add CRT Component)
IND@	Pop for India Sku

DAX



PCB  
Part Number = DA6001JC000  
PCB LA-C811P REV0 M/B 4

ZZZ1

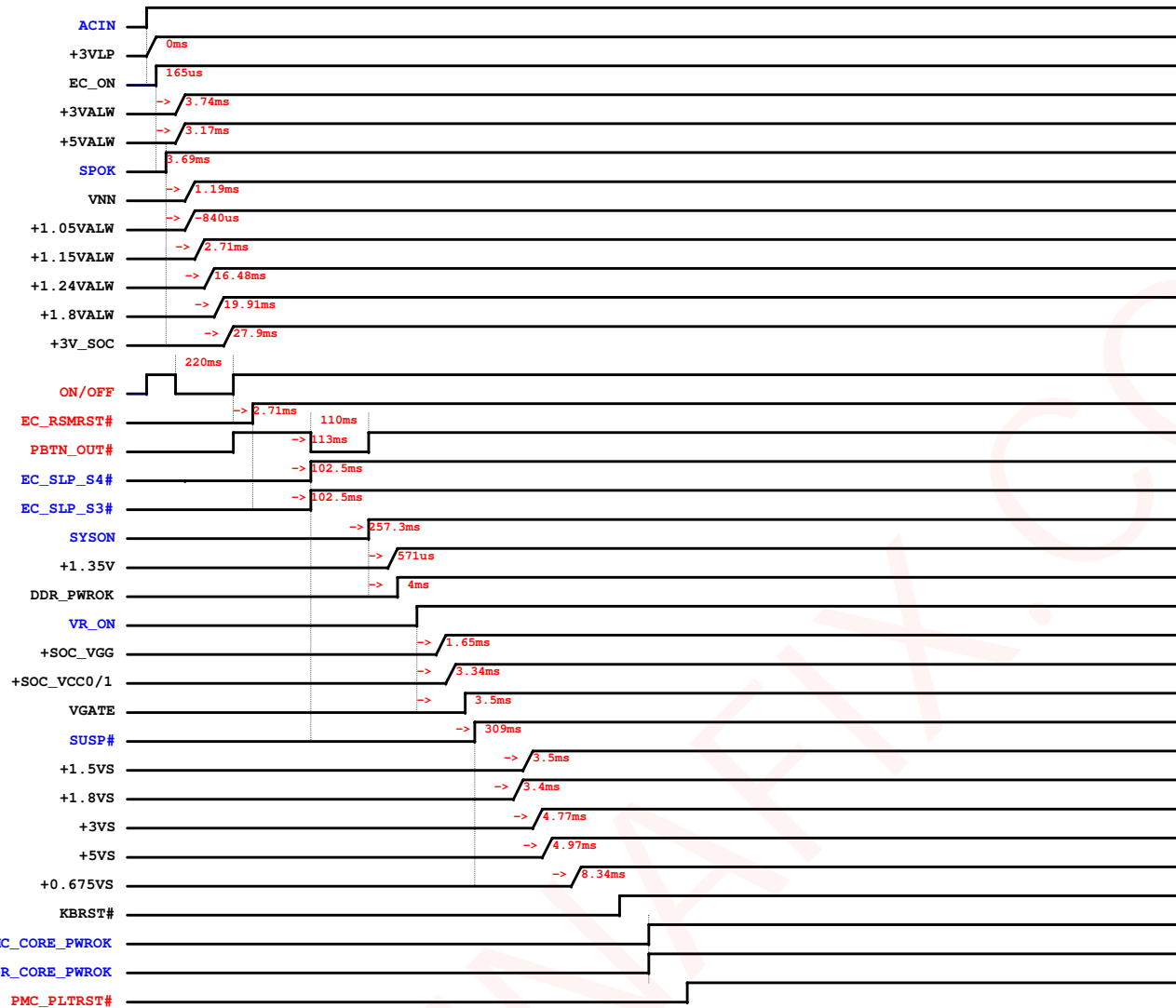


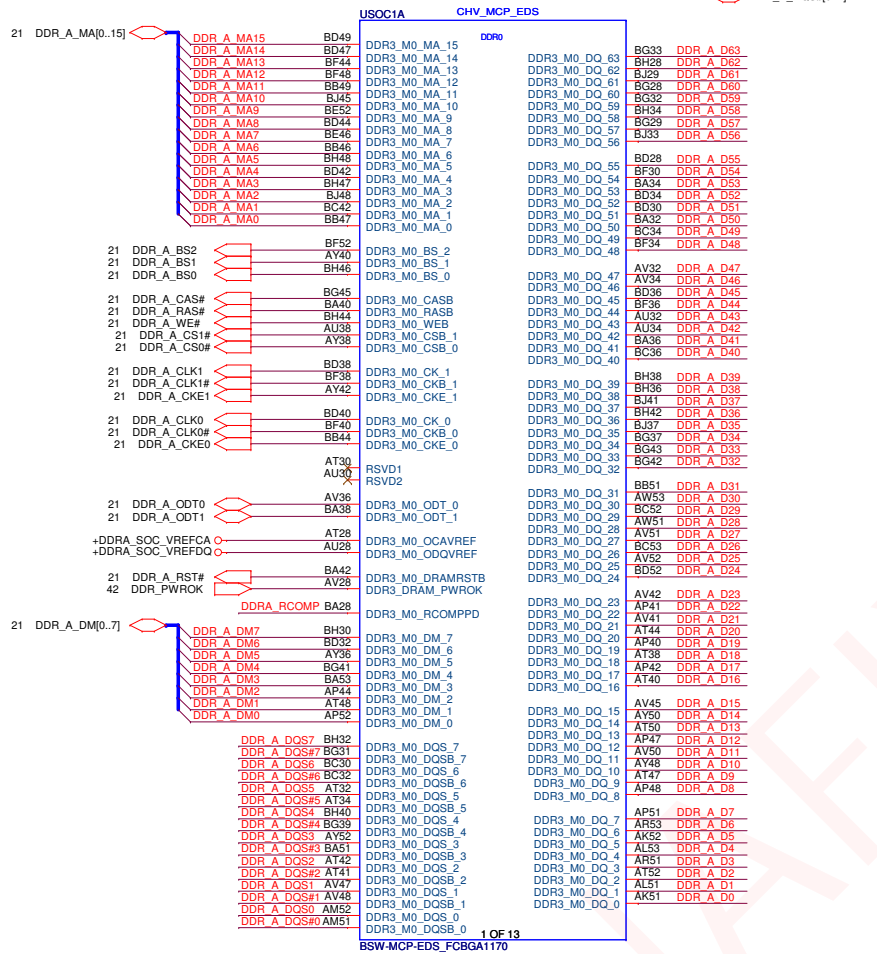
HDMI  
Part Number = RO0000003HM  
PCB 102 LA-B151P REV0 M/B 3  
45@

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SOC

G3->S0

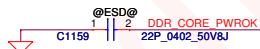
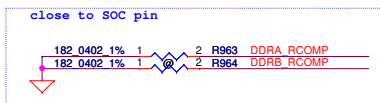




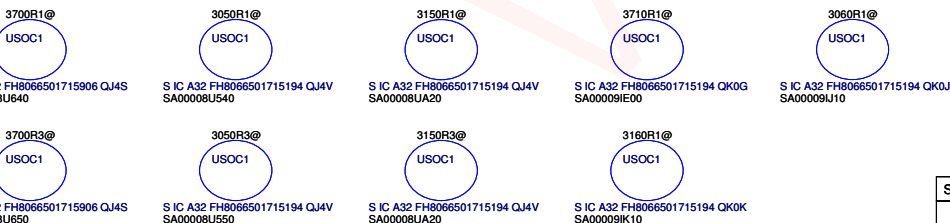
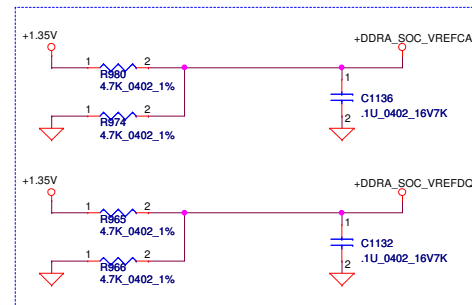
9 DDR\_CORE\_PWROK

DDRB\_RCOMP BA26

2 OF 13  
BSW-MCP-EDS\_FCBGA1170

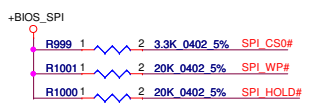
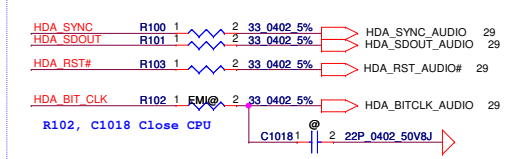


Close To SOC Pin



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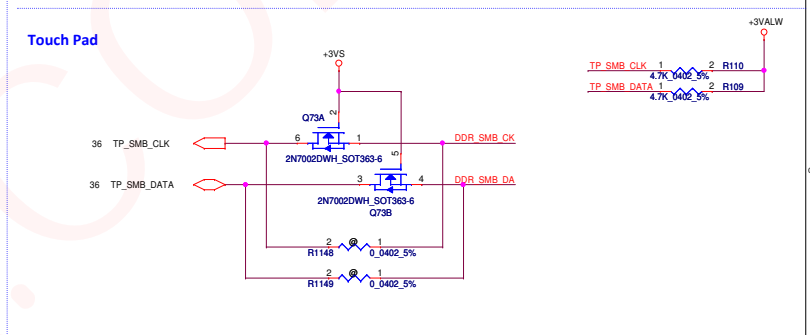
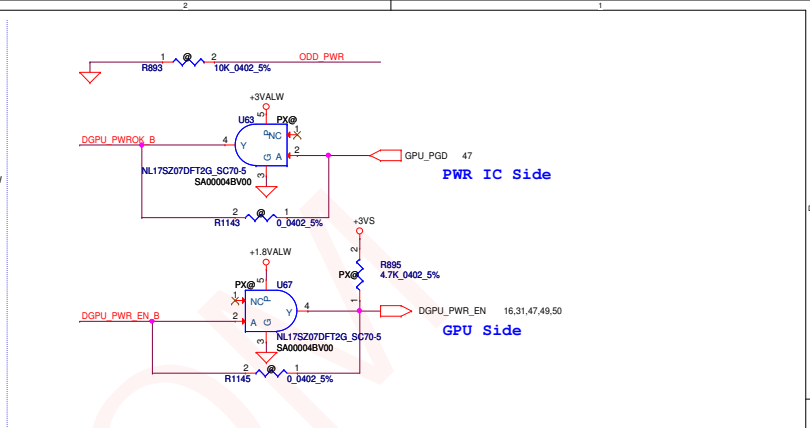




CPU SOC\_SPI\_CS0# R2581 1 AUTO@ 2 33\_0402 5% SOC\_EC\_CS0# 31  
SOC\_SPI\_CLK R2580 1 AUTO@ 2 10\_0402 5% SOC\_EC\_CLK 31  
R2587 1 NAT@ 2 SPI\_CS0#  
R2586 1 NAT@ 2 SPI\_CLK 33\_0402 5% SPI ROM  
10\_0402 5%

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>VLV-M SOC SATA/PCI-E/HDA</b>	
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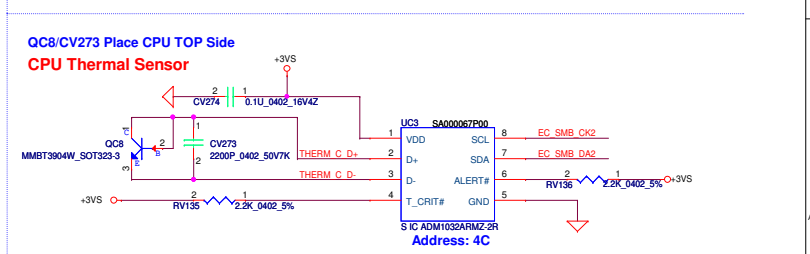
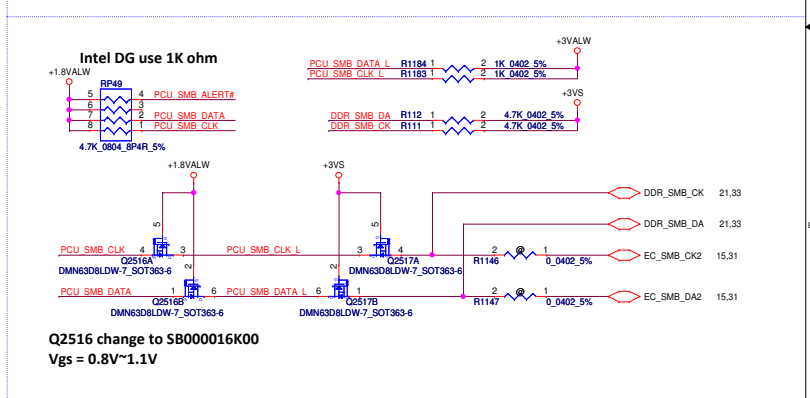
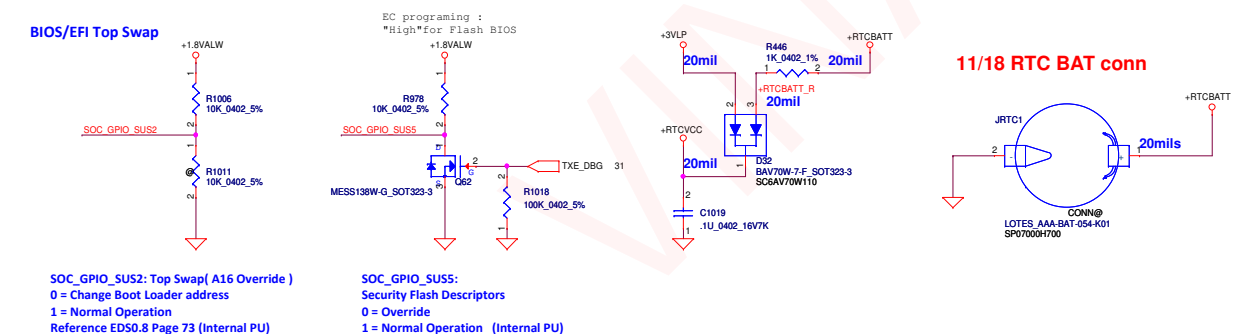
**SOC\_GPIO\_SUS4:**  
BIOS Boot Selection  
1 = LPC  
(internal PU)

+1.8VAILW

R977 1 2 100K 0402 5% SOC\_GPIO\_SUS4  
R1009 1 2 10K 0402 5% SOC\_GPIO\_SUS11  
R1008 1 2 10K 0402 5% DGPU\_PWR\_EN\_B  
R1015 1 2 10K 0402 5% SERIF

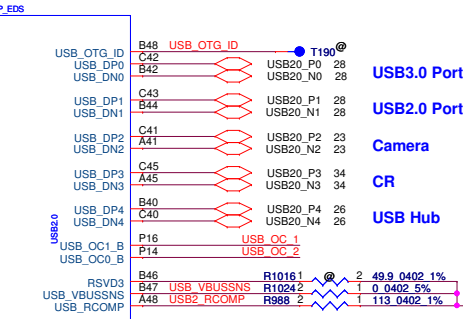
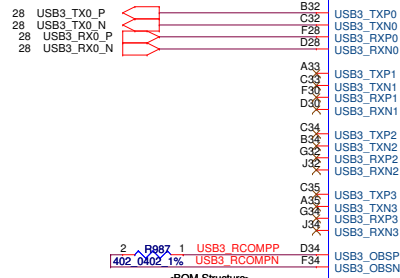
R992 1 2 10K 0402 5% DGPU\_PWROK\_B  
R1029 1 2 4.7K 0402 5% SOC\_GPIO\_SUS8  
R1010 1 2 4.7K 0402 5% PX0

+1.8VAILW

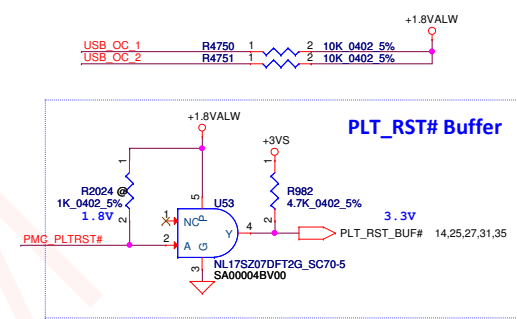




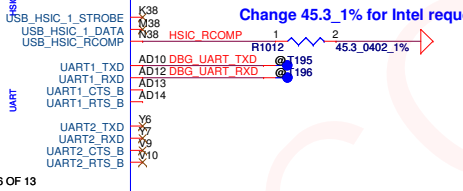
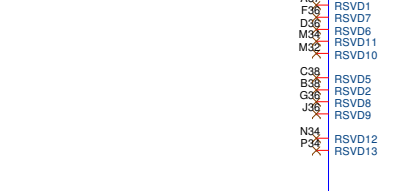
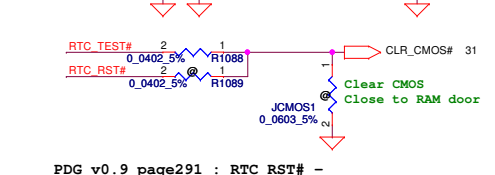
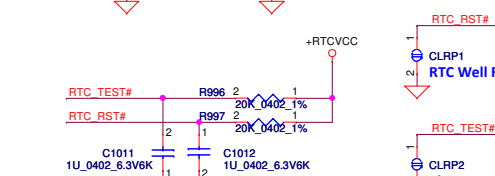
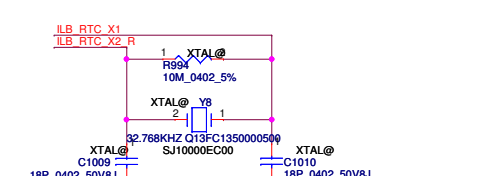
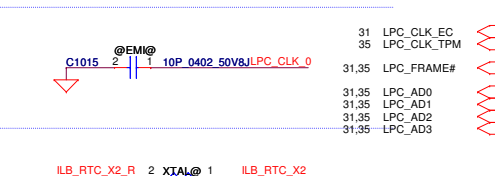
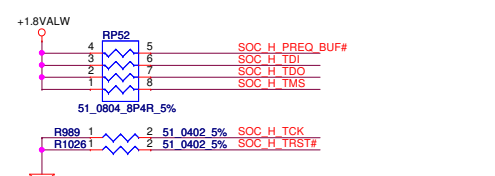
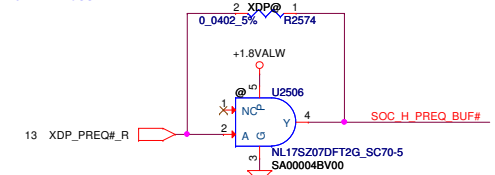
# USB3 Port 0



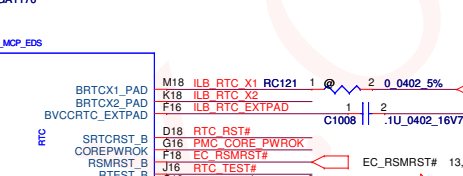
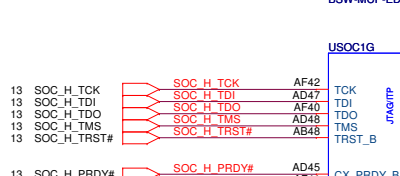
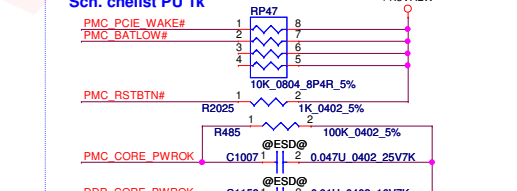
# USB3.0 Port USB2.0 Port Camera CR USB Hub



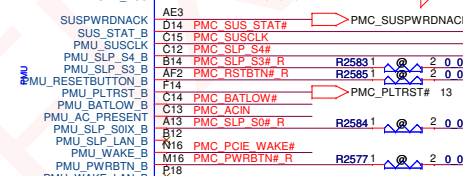
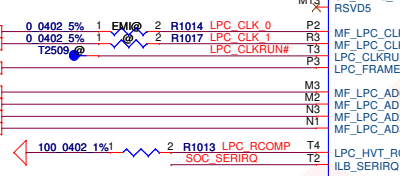
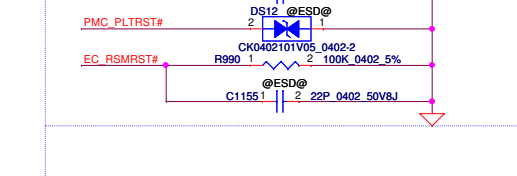
For XDP use



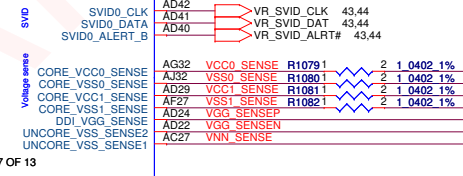
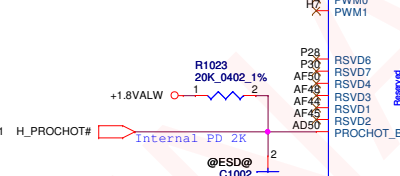
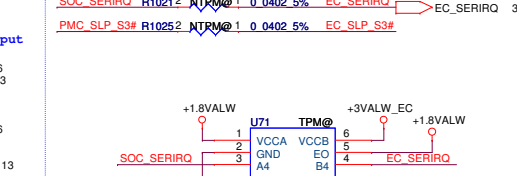
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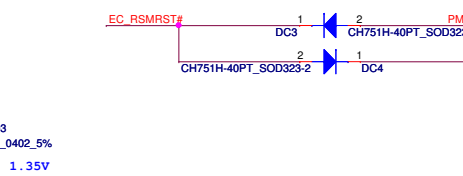
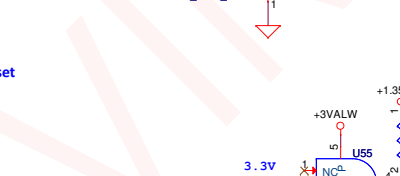
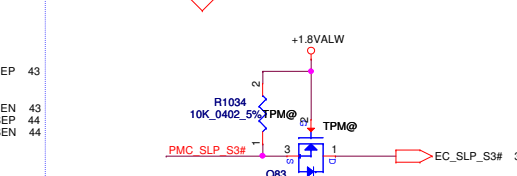
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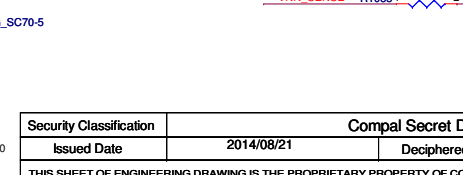
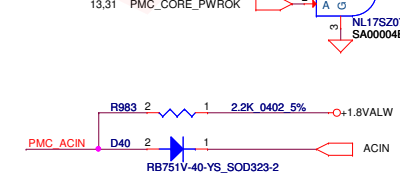
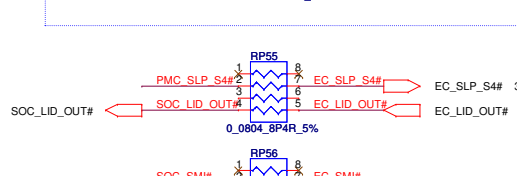
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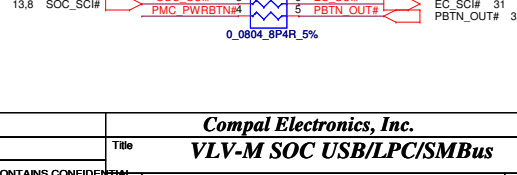
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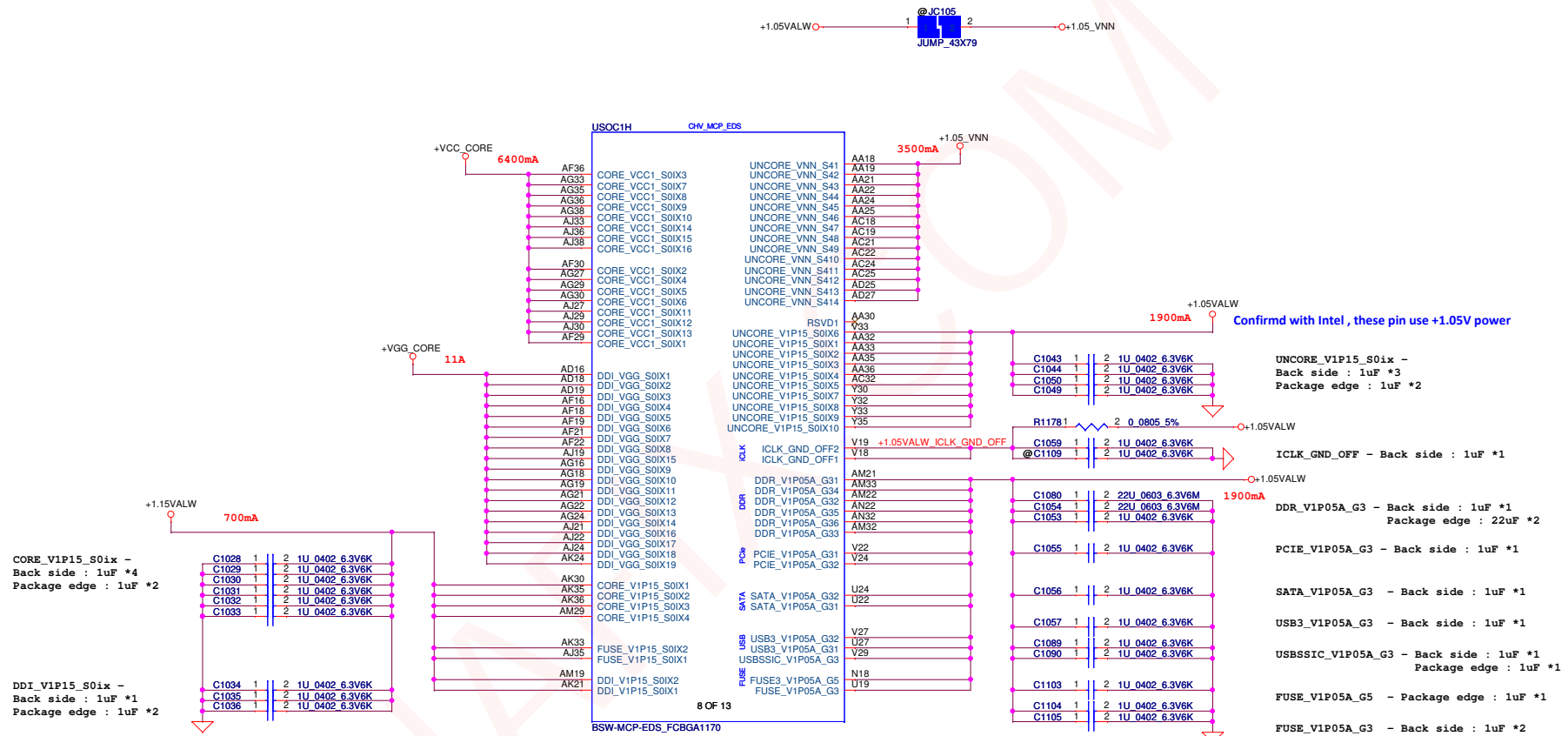


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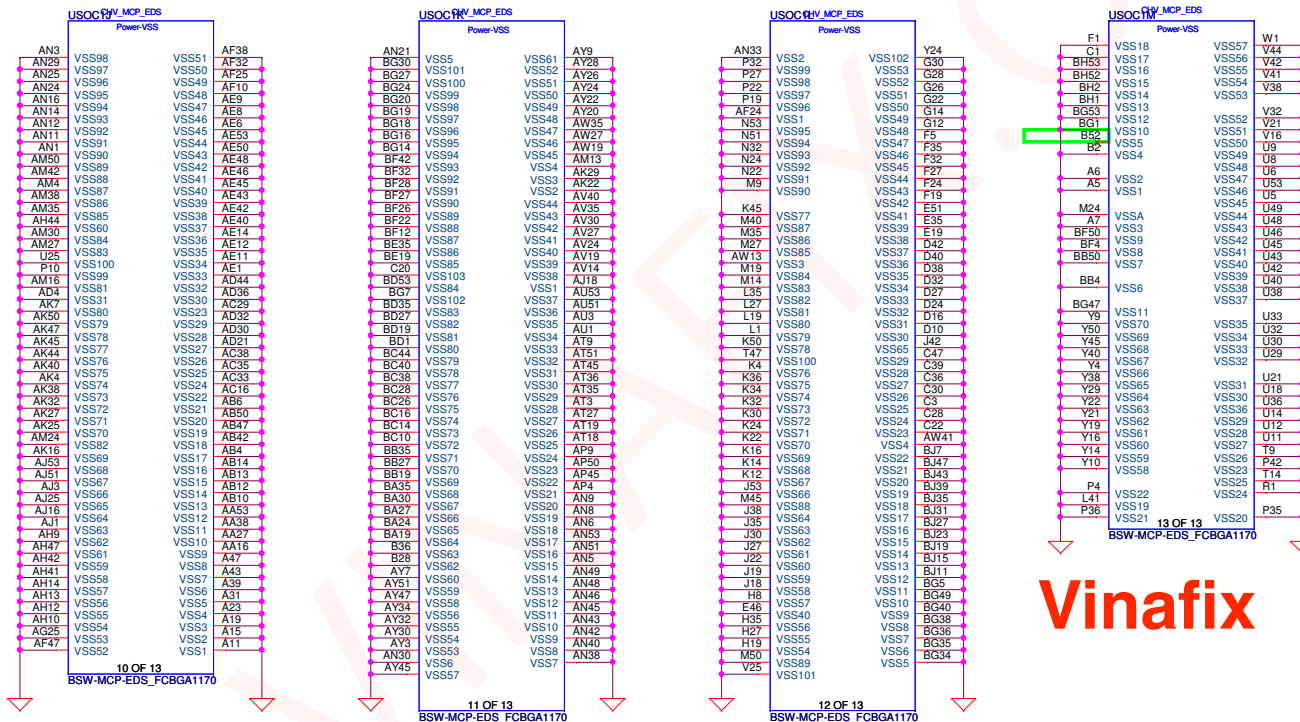


PDG v0.9 page291 : RTC\_RST# -  
When asserted, this signal resets register bits in the RTC well.

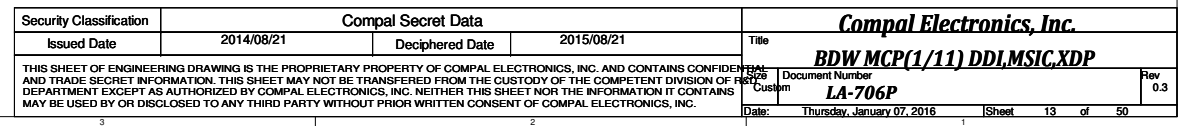
Security Classification		Compal Secret Data		Title	
Issued Date	2014/08/21	Deciphered Date	2015/08/21	VIV-M SOC USB/LPC/SMBus	
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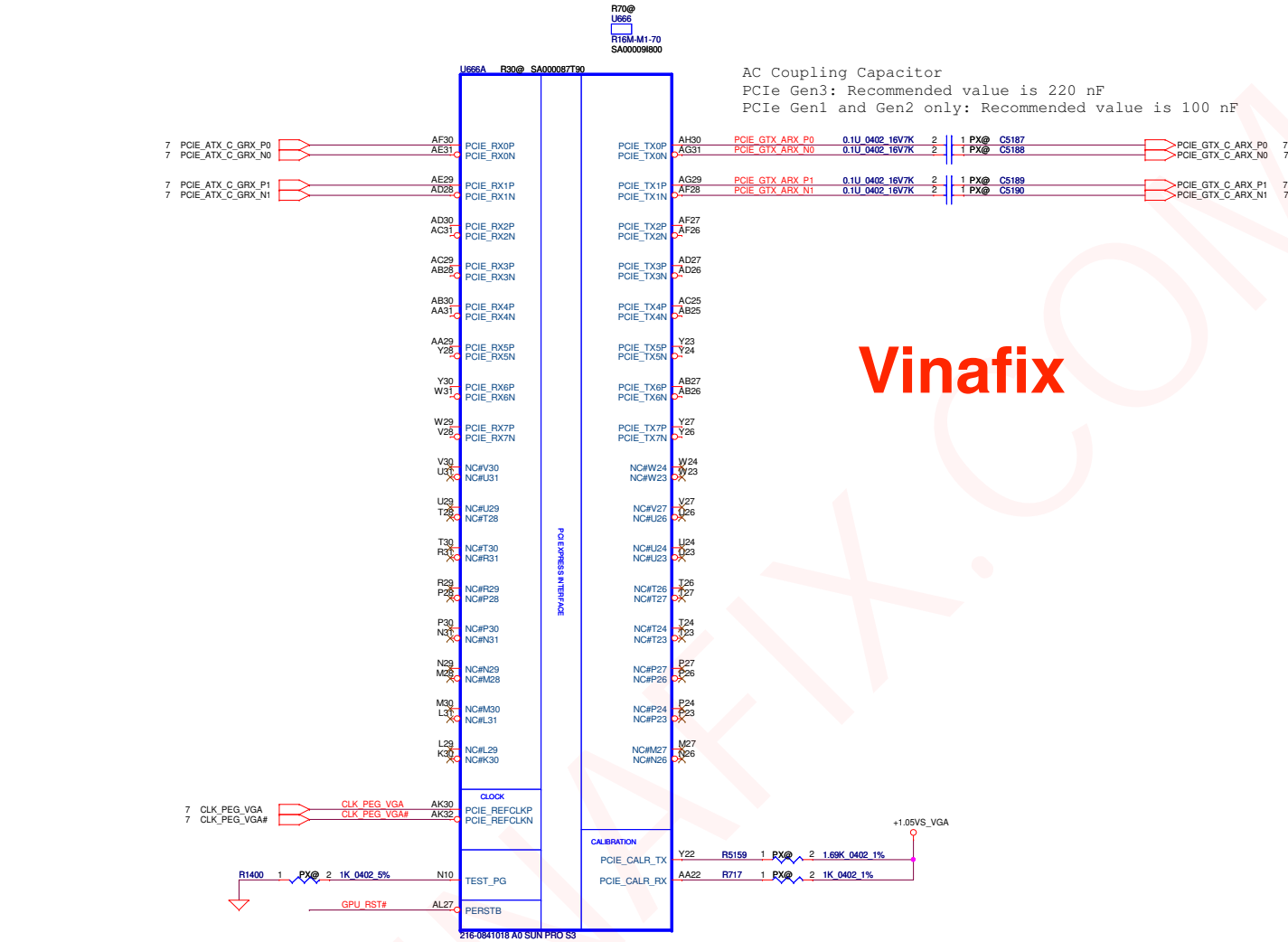






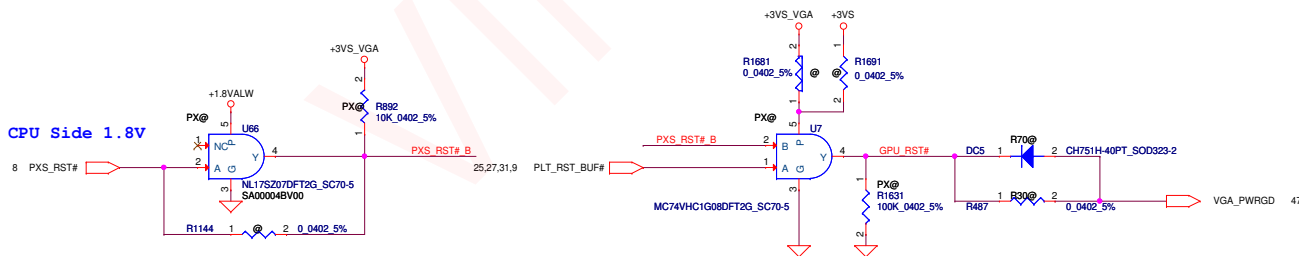
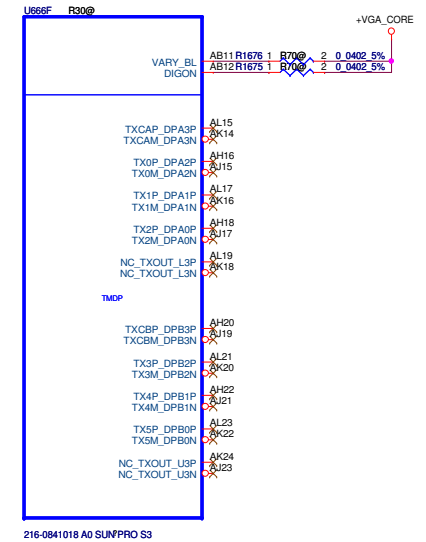
## XDP CONN





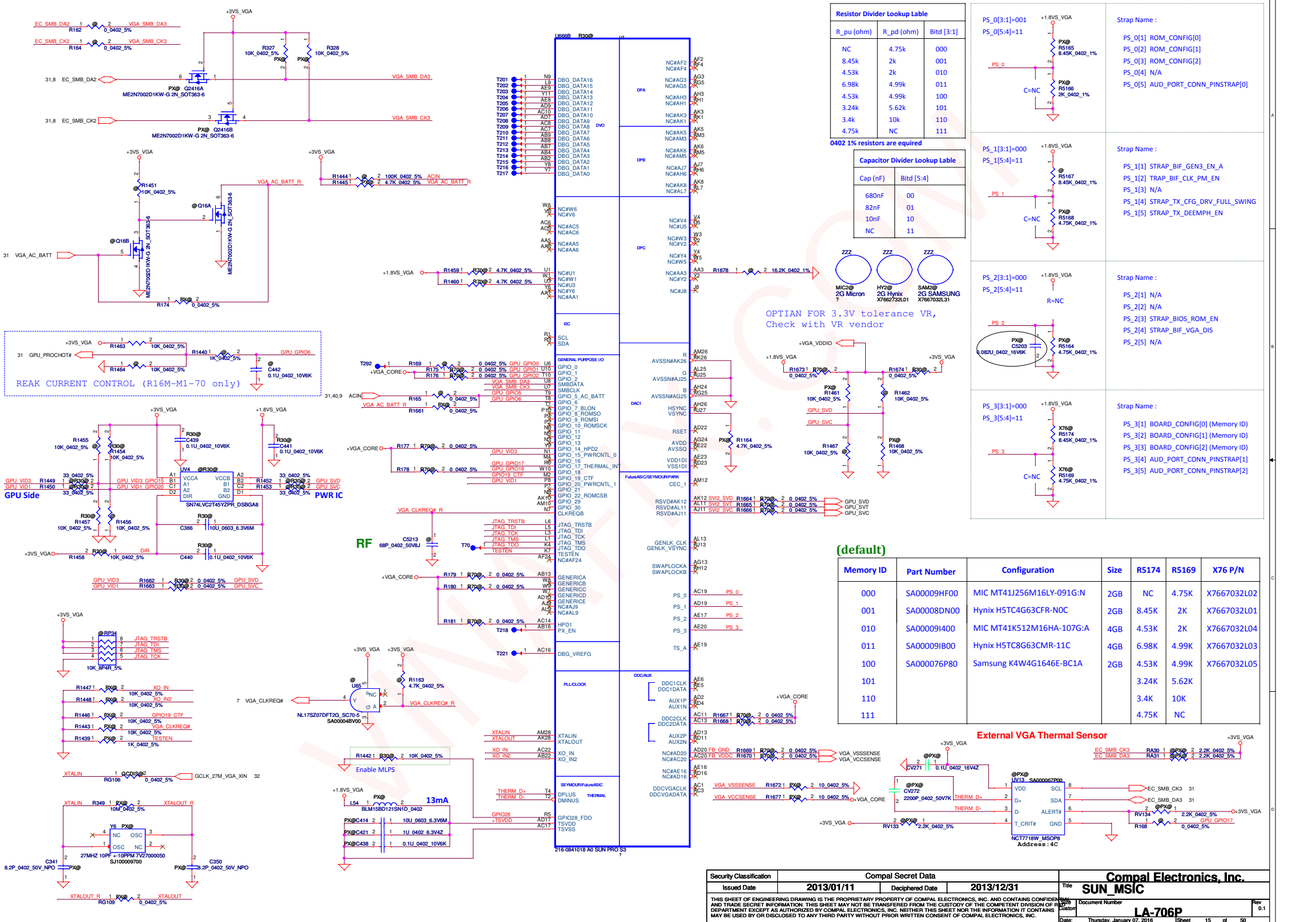
Vinafix

No Use GPU Display Port output



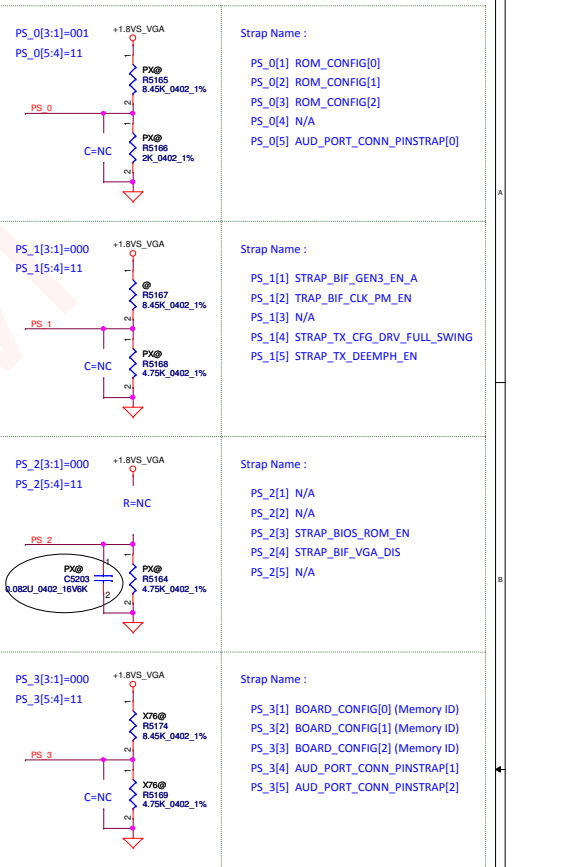
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	SUN PCIe/DP	
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Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



Memory ID	Part Number	Configuration	Size	R5174	R5169	X76 P/N
000	SA0009HF00	MIC MT41J256M16LY-091G:N	2GB	NC	4.75K	X7667032L02
001	SA0008DN00	Hynix H5TC4G63CFR-NOC	2GB	8.45K	2K	X7667032L01
010	SA0009I400	MIC MT41K512M16HA-107G:A	4GB	4.53K	2K	X7667032L04
011	SA0009I800	Hynix H5TC8G63CMR-11C	4GB	6.98K	4.99K	X7667032L03
100	SA00076P80	Samsung K4W4G1646E-BC1A	2GB	4.53K	4.99K	X7667032L05
101				3.24K	5.62K	
110				3.4K	10K	
111				4.75K	NC	

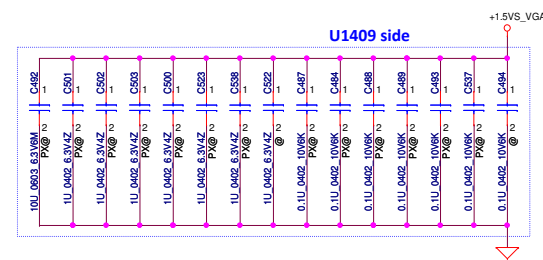
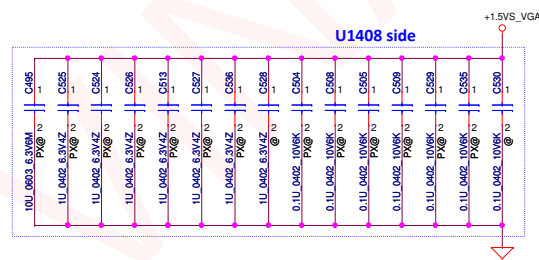
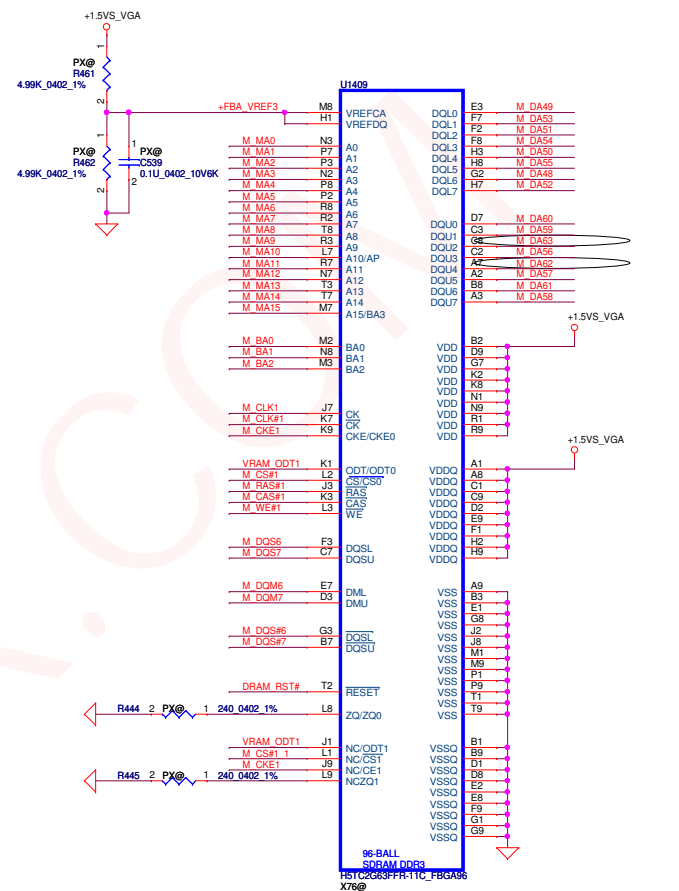
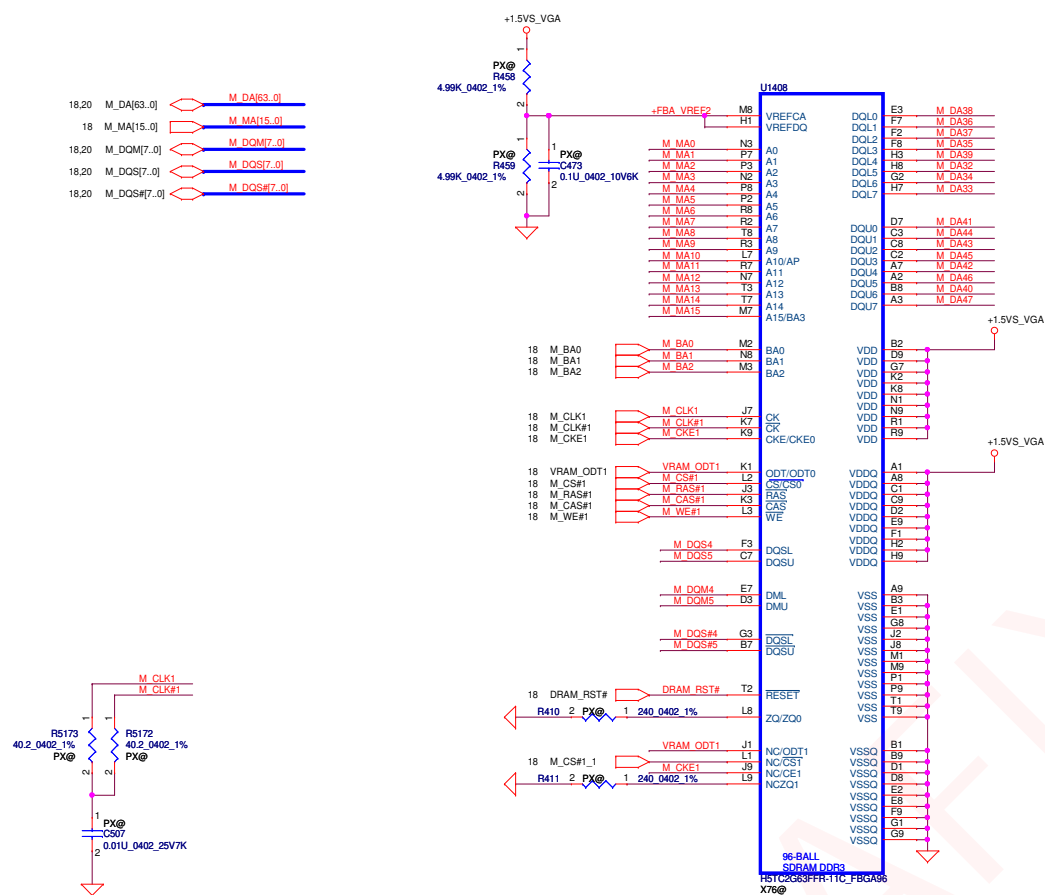








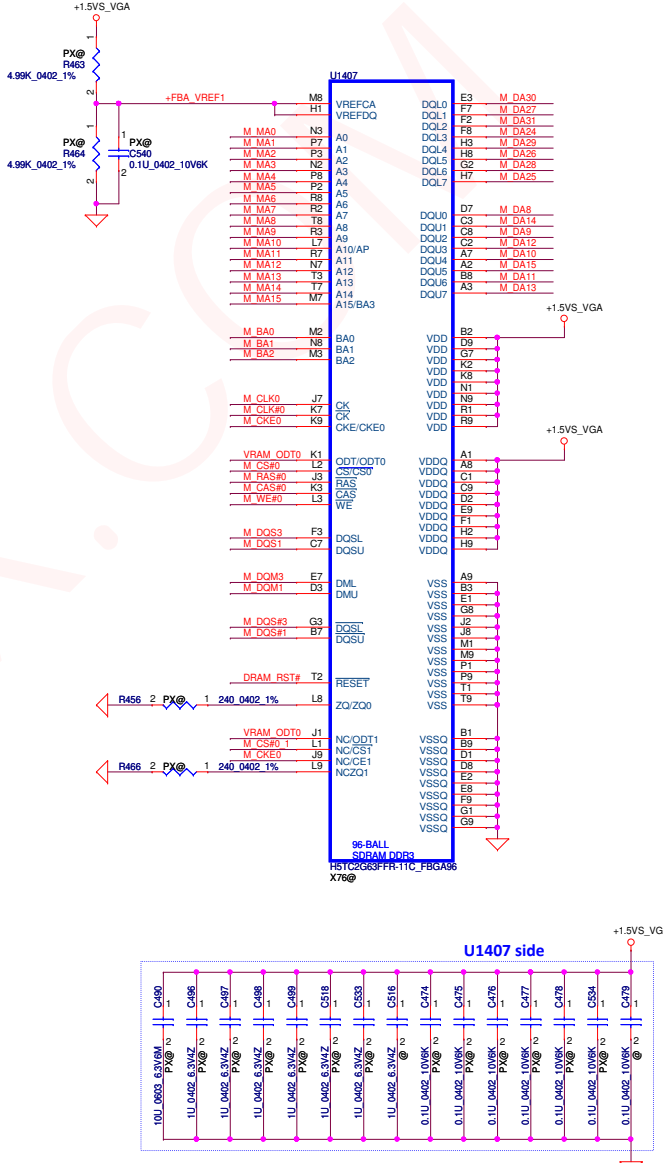
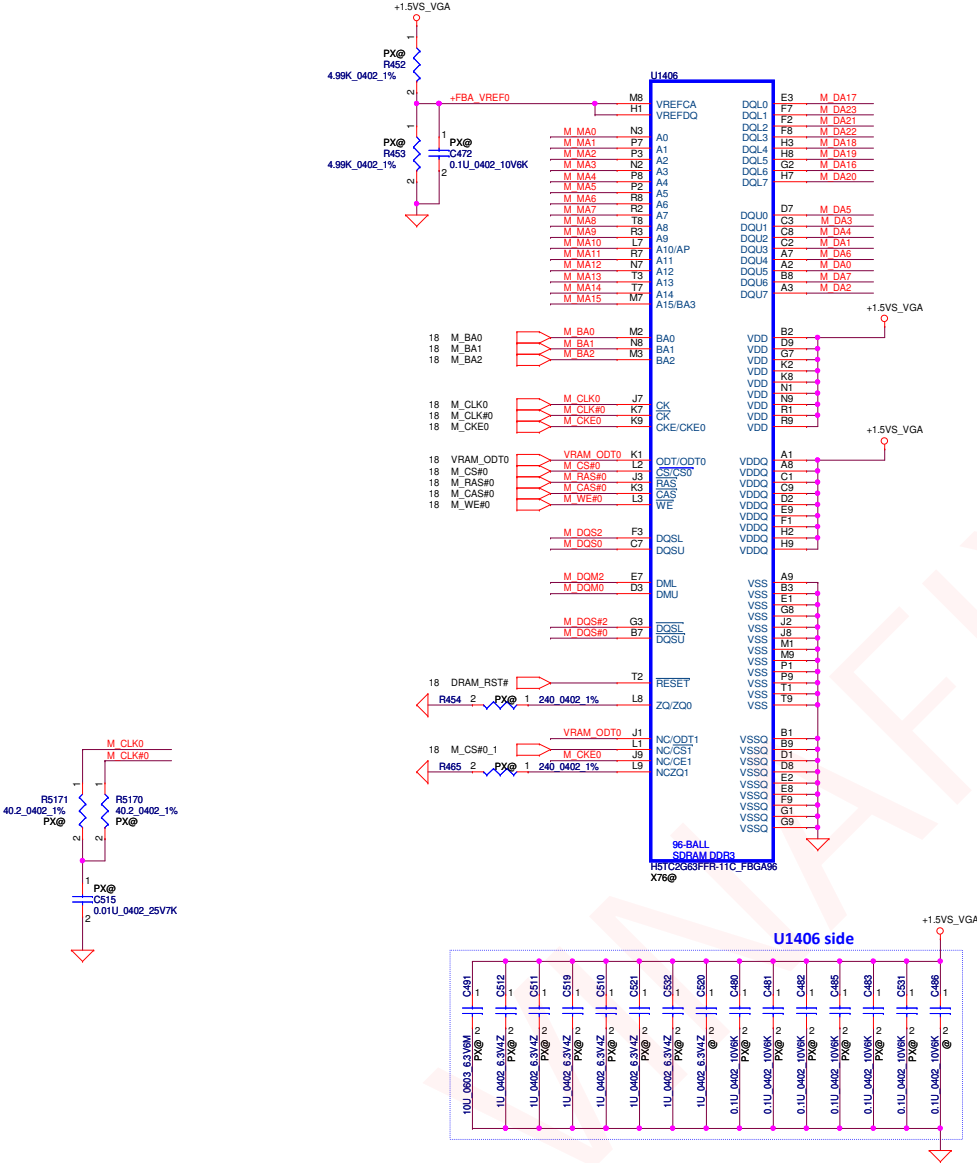
1	2
Memory Partition A - Upper 32 bits	



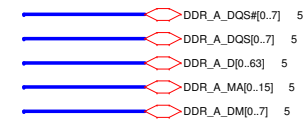
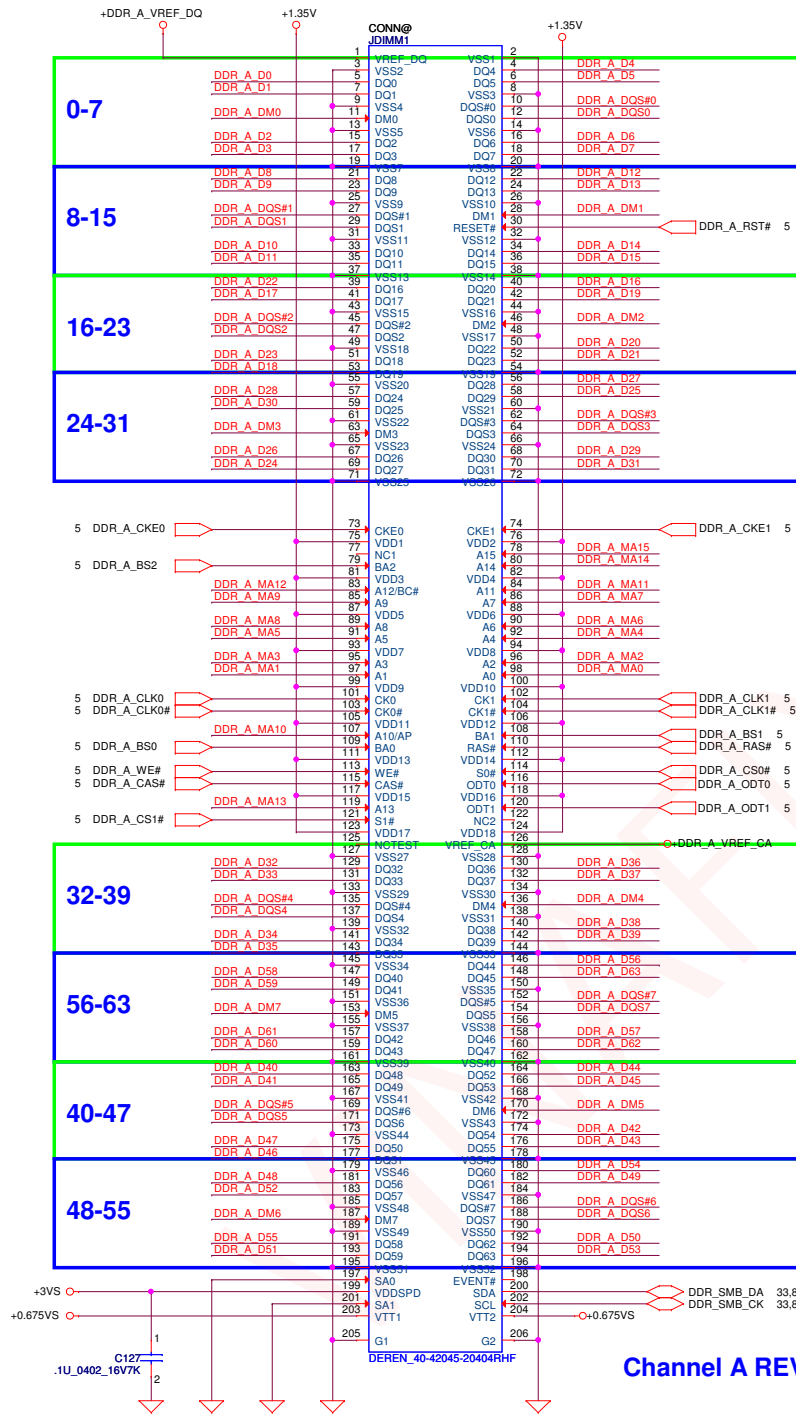
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2013/01/11	Deciphered Date	2013/12/31	Title
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		Size Document Number		Rev 0.1	
		Date: Thursday, January 07, 2016		Sheet 19 of 50	

Memory Partition A - Lower 32 bits

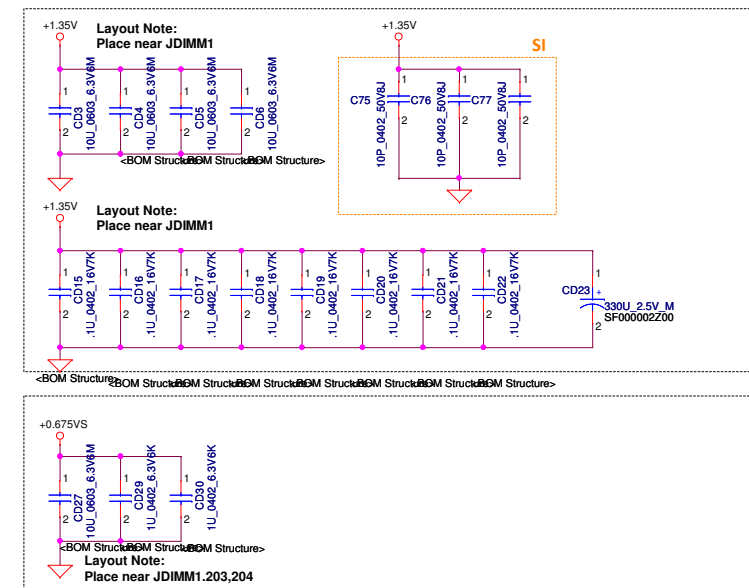
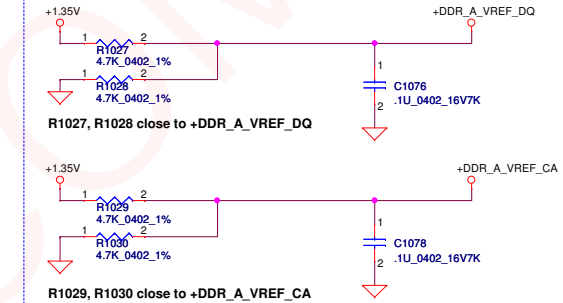
- 18,19 M\_DA[63..0] M\_DA[63..0]
- 18 M\_MA[15..0] M\_MA[15..0]
- 18,19 M\_DQM[7..0] M\_DQM[7..0]
- 18,19 M\_DQS[7..0] M\_DQS[7..0]
- 18,19 M\_DQS#[7..0] M\_DQS#[7..0]



All VREF traces should have 10 mil trace width



Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO  
DIMMS ON DIMM\_VREF\_CA / DIMM\_VREF\_DQ  
Decoupling caps are needed; one 0.1  $\mu$ F placed close to VREF pins of each DDR3 SODIMM.



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				Customer	1.0
				Date: Thursday, January 07, 2016	Sheet 21 of 50

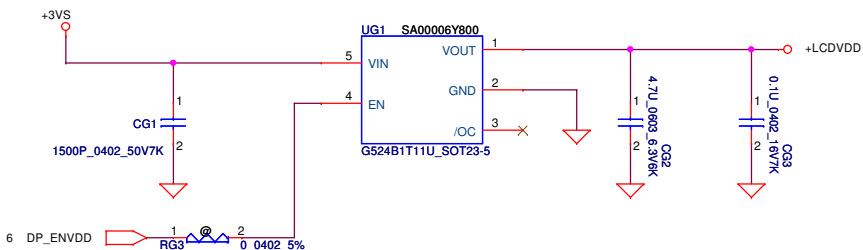
<Address: SA0:SA1=10 (A2H)>  
DIMM\_2 REV H:4mm

Channel B Rev

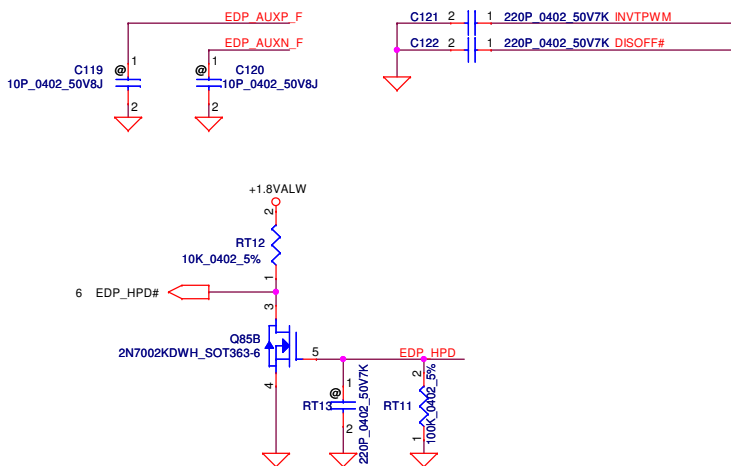
Security Classification	Compal Secret Data			Title		
Issued Date	2014/08/21	Deciphered Date	2015/08/21	DDR3L DIMMB		
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				LA-706P		0.1
				Date: Thursday, January 07, 2016		Sheet 22 of 50



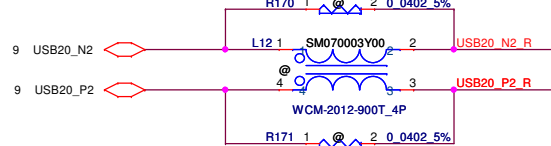
## LCD Power Switch



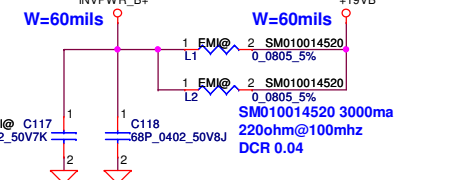
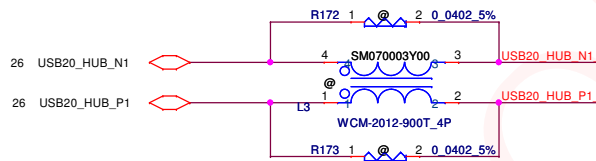
## CC119/110 close JLVDS1



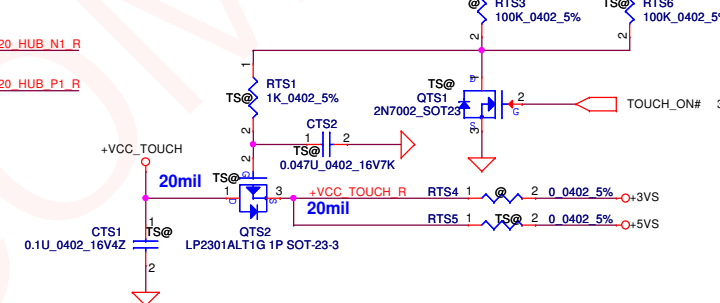
## Camera



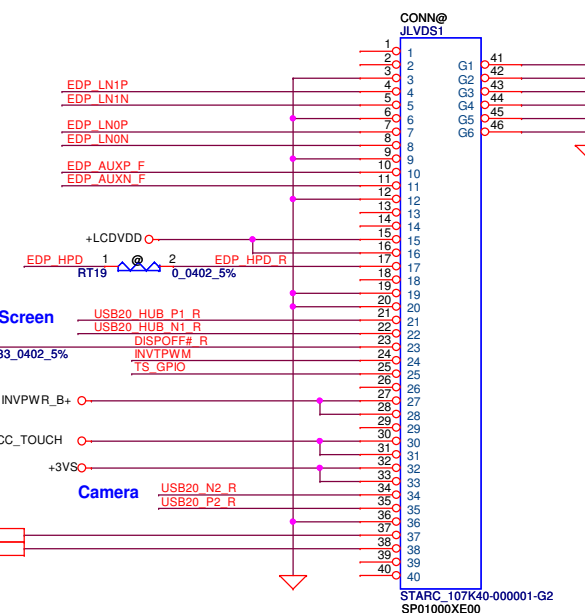
## Touch Screen



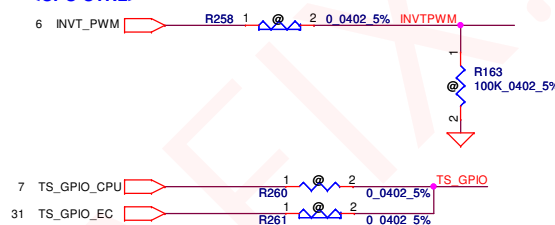
## Touch Screen Power



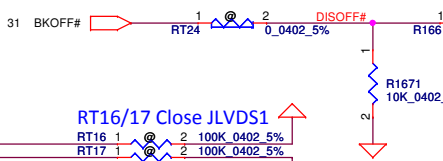
## LCD PANEL Conn.



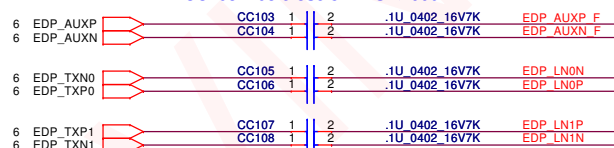
## <CPU CTRL>



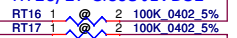
## <EC CTRL>



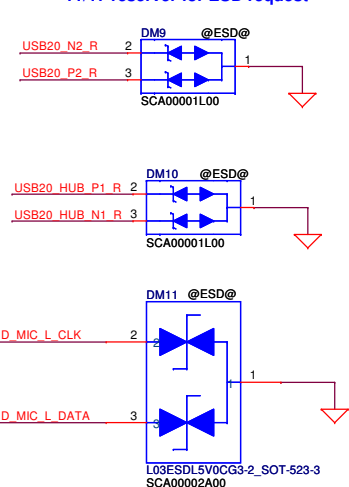
## CC103~108 close JLVDS1



## RT16/17 Close JLVDS1

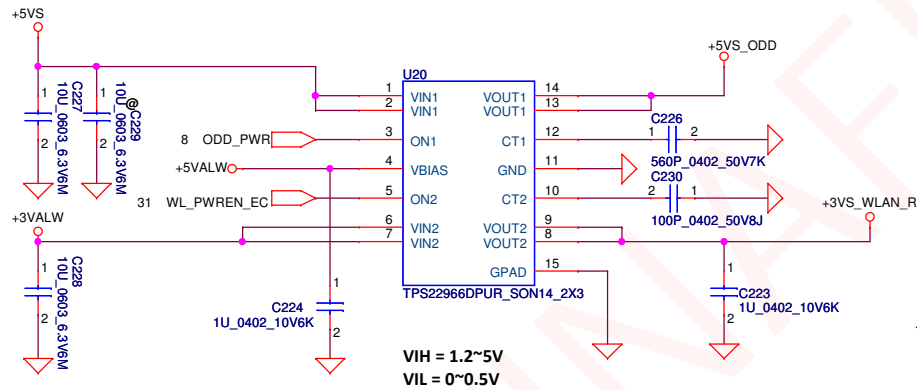
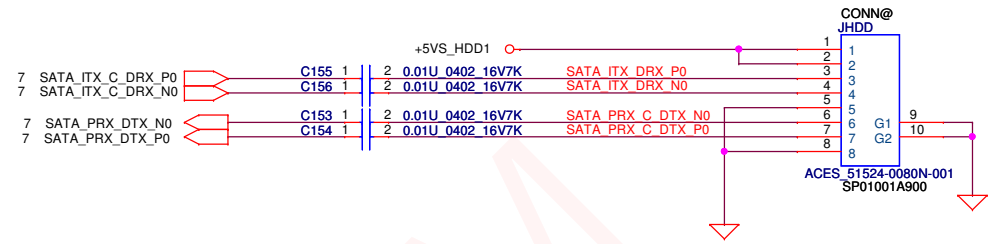
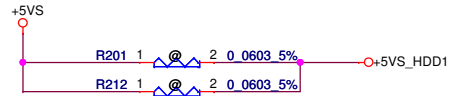


## 11/17 reserver for ESD request

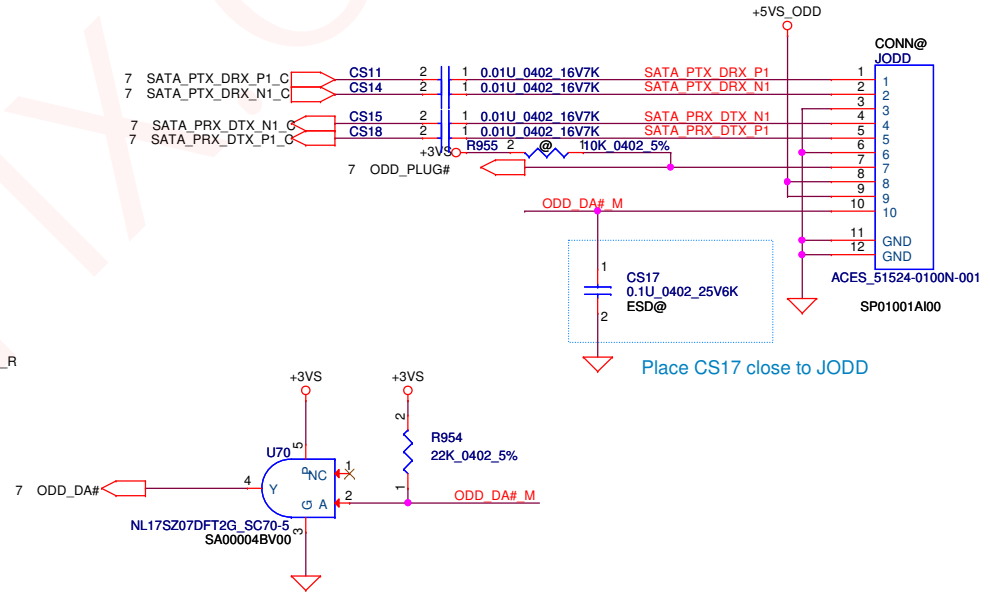


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Size	Document Number	Rev		0.1	
Date:	Thursday, January 07, 2016	Sheet	23	of	51

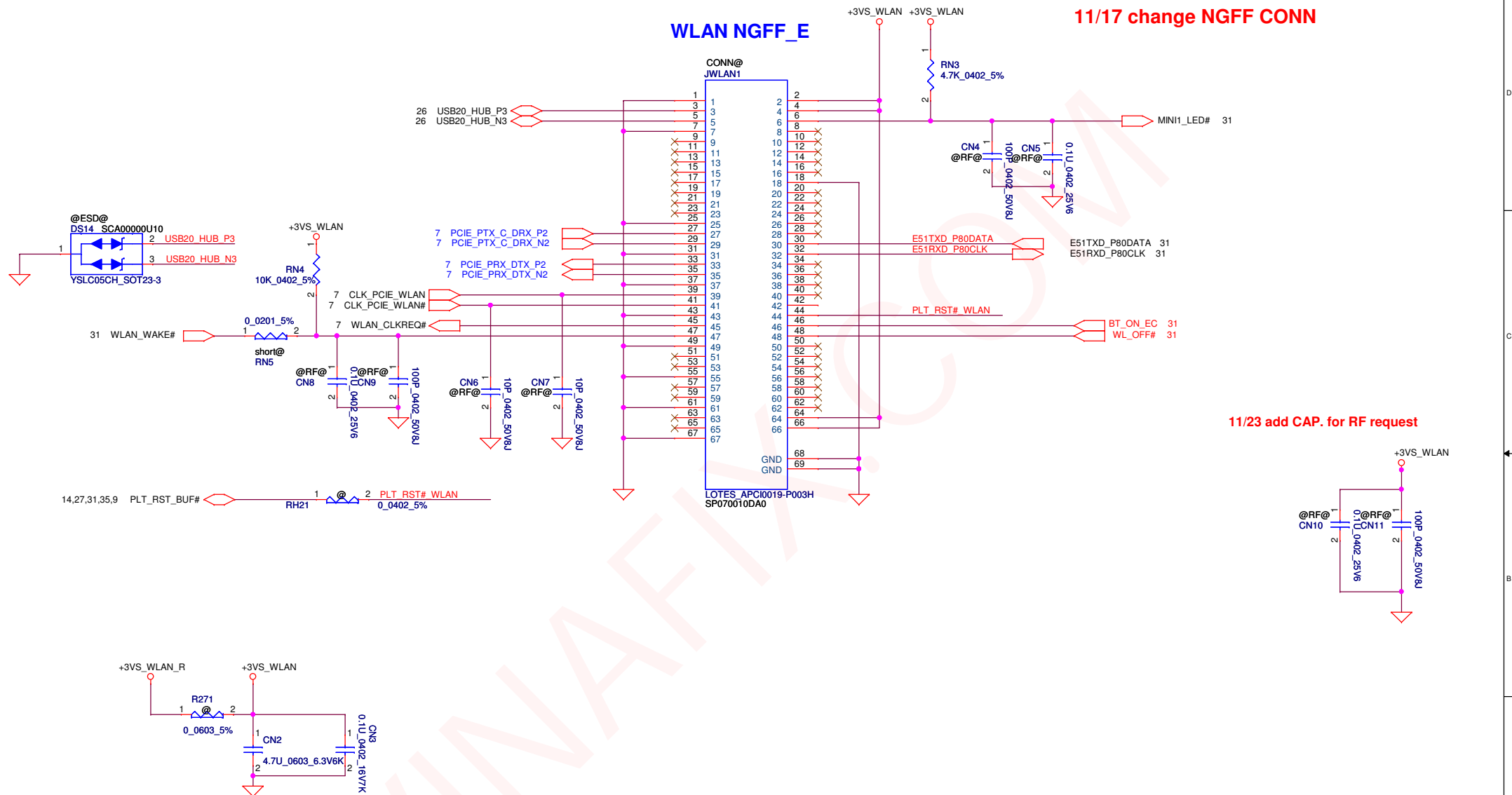
## 2.5" SATA HDD connector



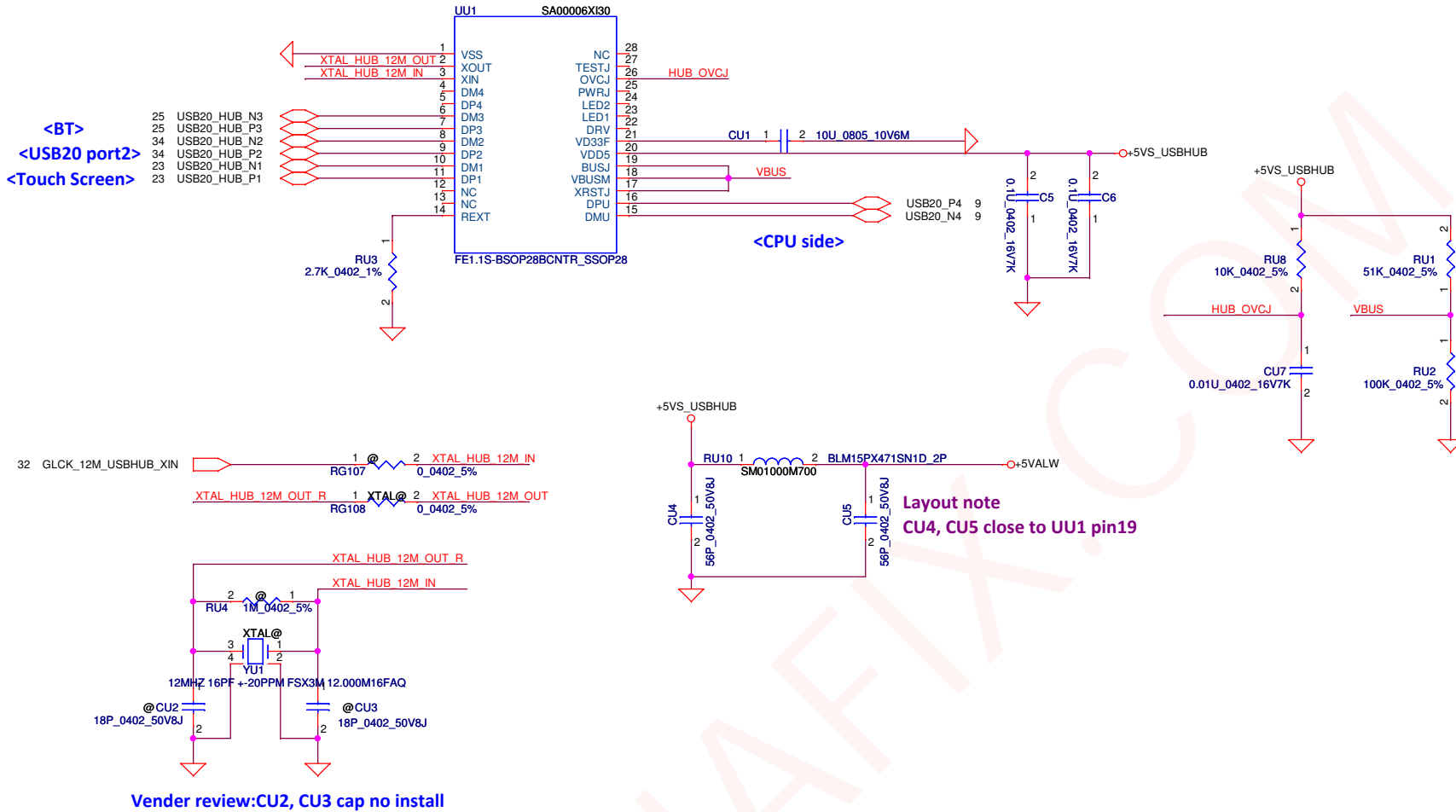
VIH = 1.2~5V  
VIL = 0~0.5V



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Thursday, January 07, 2016
				Sheet	24 of 51

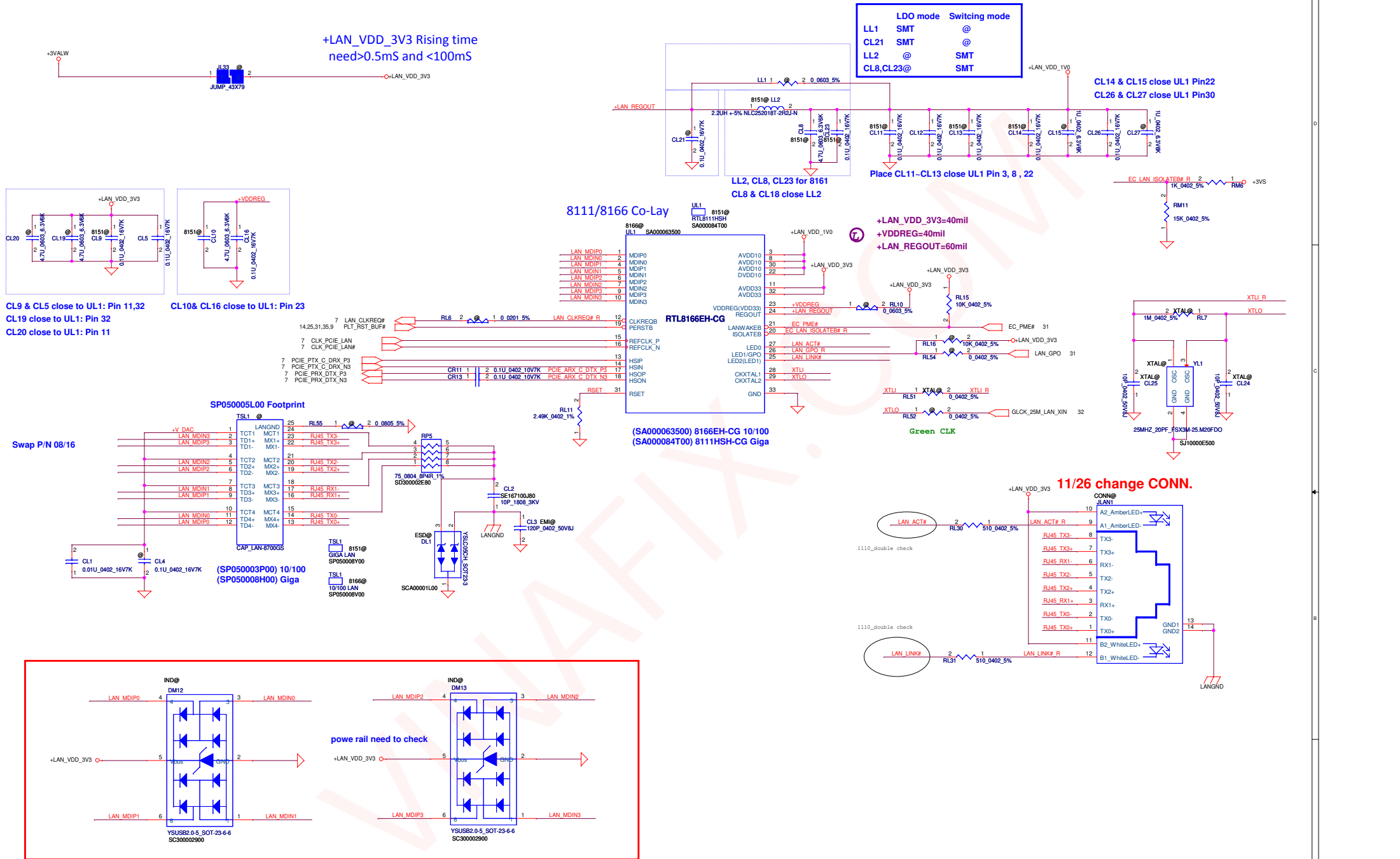


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				LA-706P	Rev 0.1
				Date: Thursday, January 07, 2016	Sheet 25 of 51

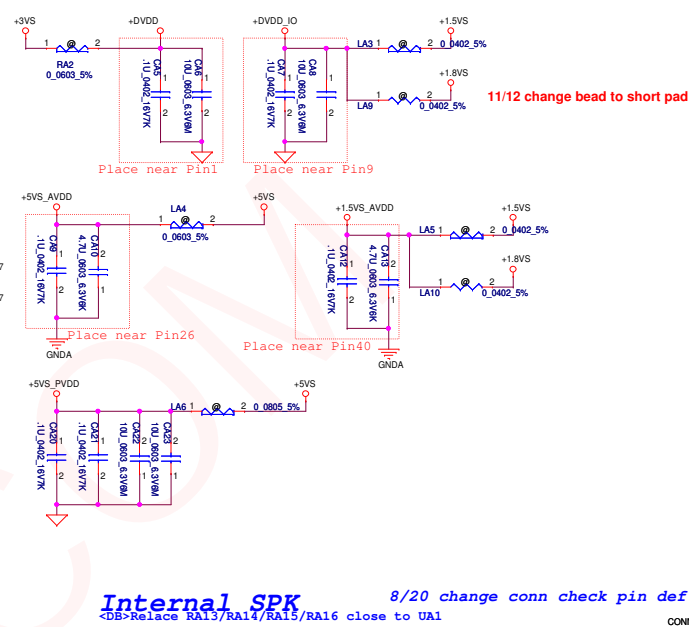


Vinafix.com

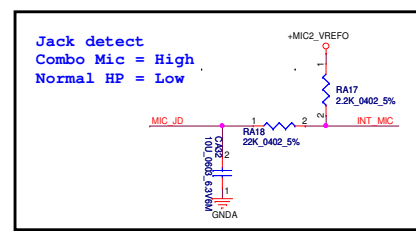
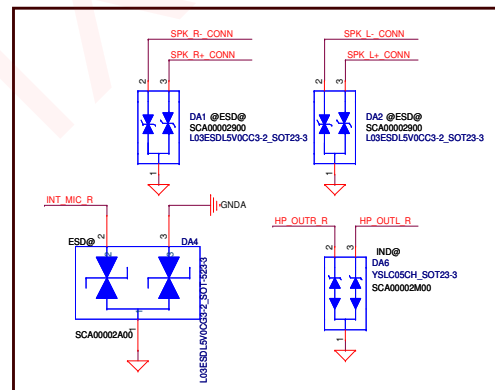
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	USB2.0 Hub
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				Date	Thursday, January 07, 2016
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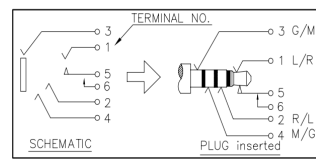
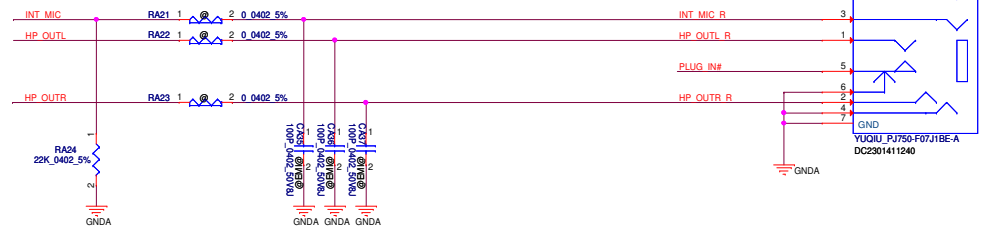




**Internal SPK**  
 <DB>Relace RA13/RA14/RA15/  
 2 0 0603 5%  
 2 0 0603 5%  
 2 0 0603 5%  
 2 0 0603 5%  
 wide 40 MIL

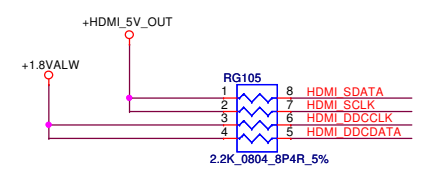
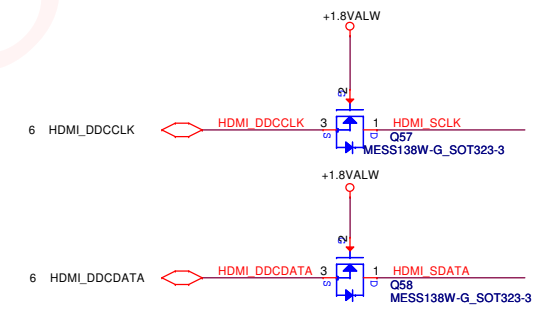
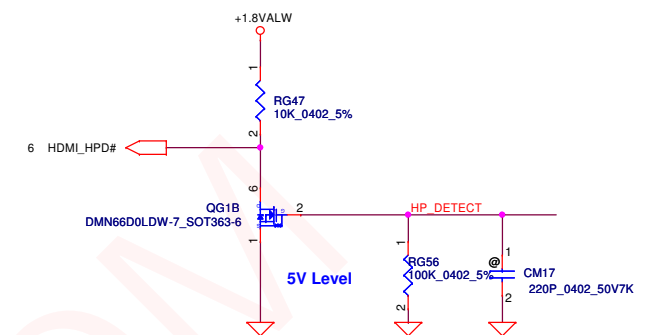
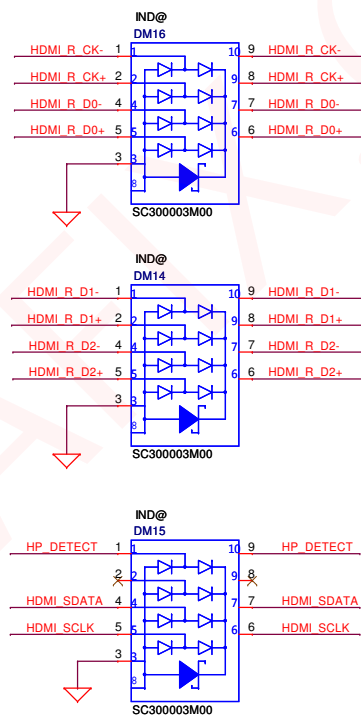
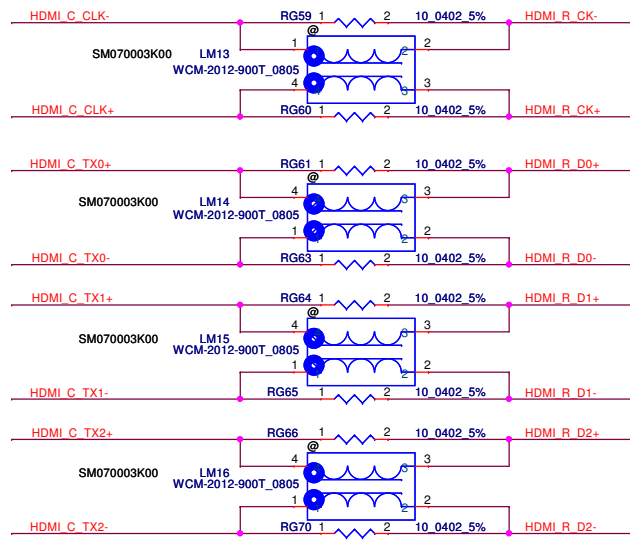
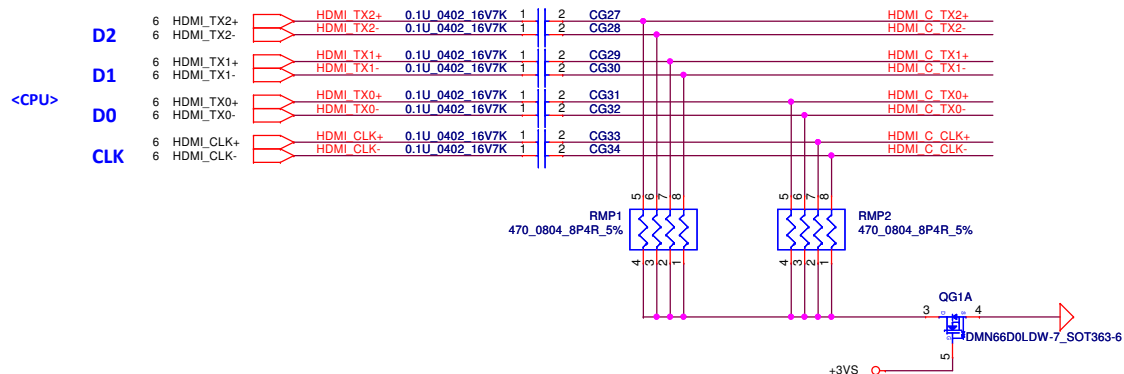


HPR, HPL, 15mil Keep 30mil

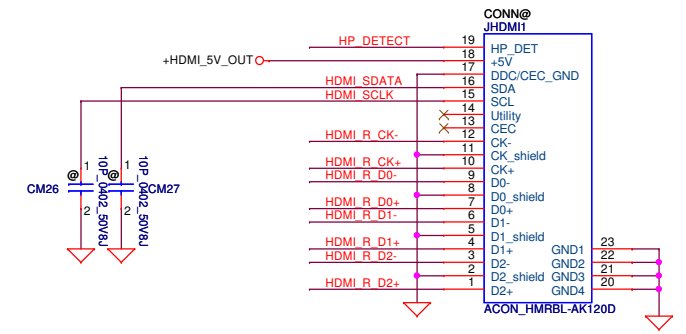
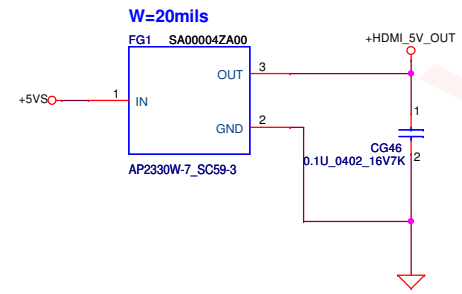


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Size	C	Document Number	LA-706P	Rev	0.1
Version		Deciphered	Rev	0.1	0.1

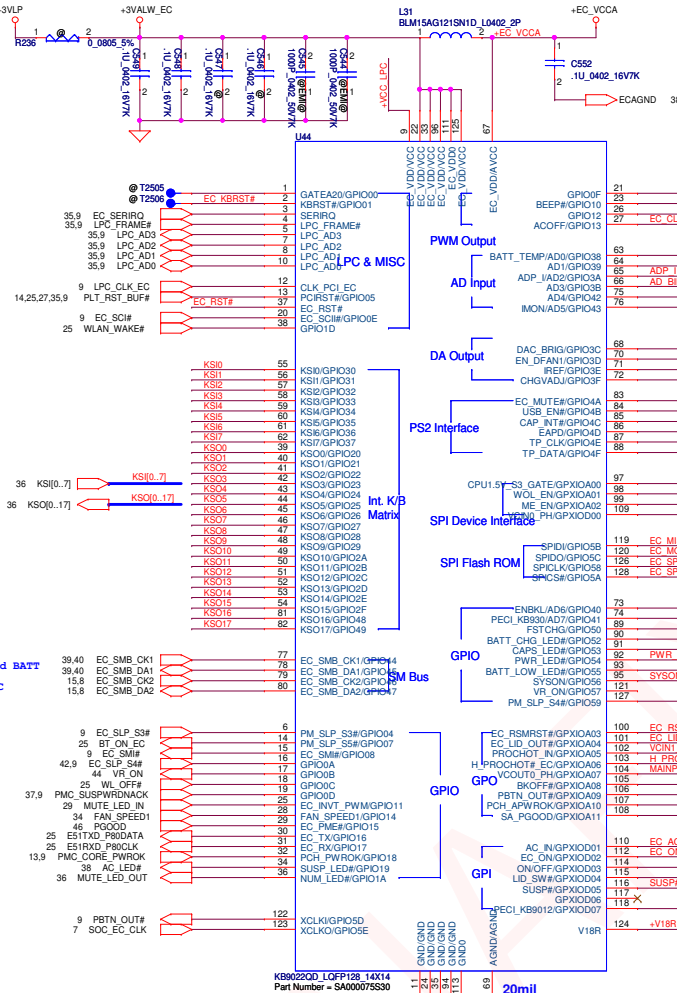
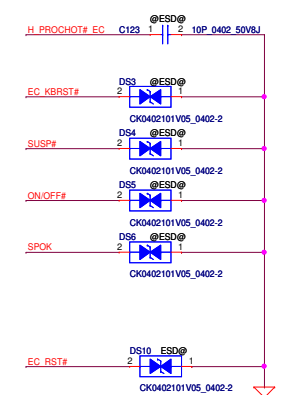
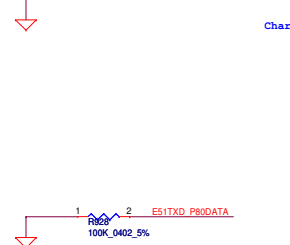
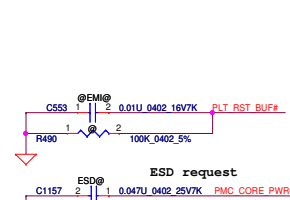
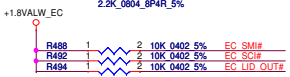
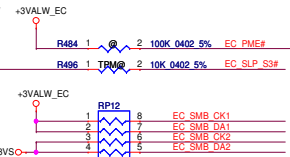
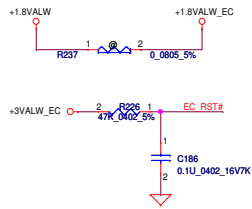




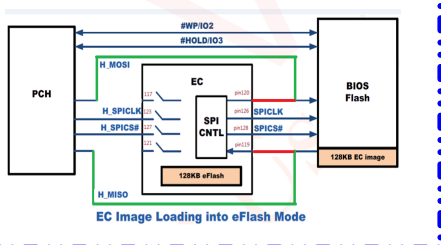
# HDMI Conn.



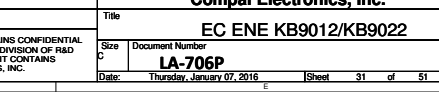
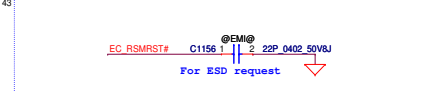
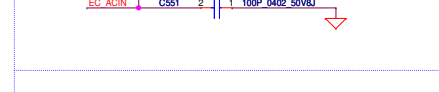
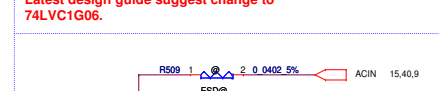
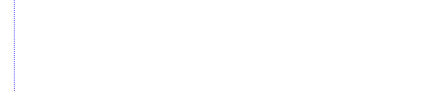
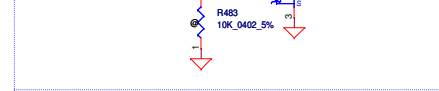
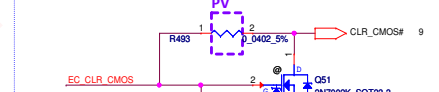
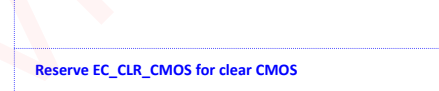
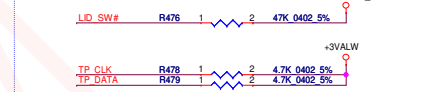
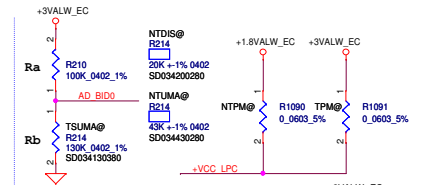
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	HDMI Conn/Level shift	
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Pin117,123,127,121 For share ROM function



NonTS	DB	SI	PV	MV
UMA R214 DIS R214	0 ohm 12k ohm	15k ohm 20k ohm	27K ohm 33k ohm	43K ohm 56k ohm
TS	DB	SI	PV	MV
UMA R214 DIS R214	75k ohm 100k ohm	130K ohm 160k ohm	200K ohm 240k ohm	270K ohm 330k ohm

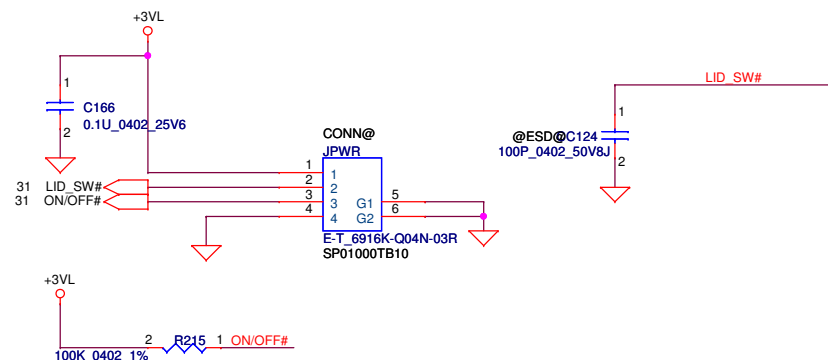


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Issued Date	2014/08/21	Deciphered Date	2015/08/21
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		LA-706P	Rev 0.1
		Date	Thursday, January 07, 2016
		Sheet	31 of 51

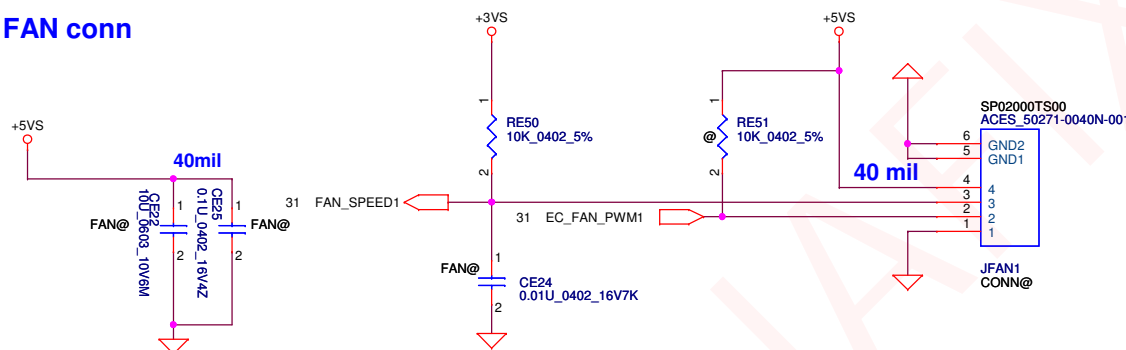




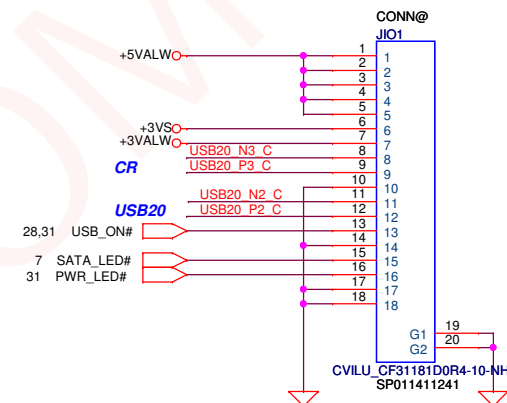
## Power Button Connector



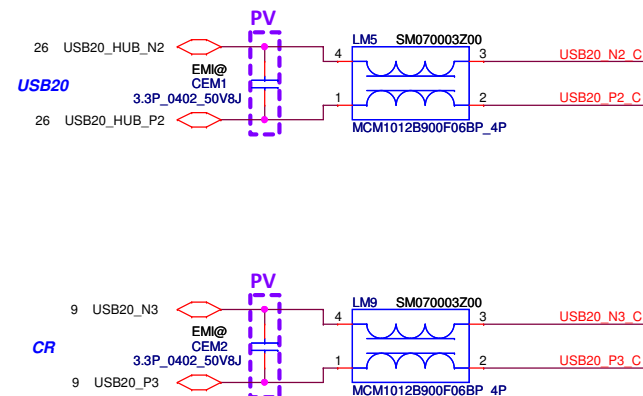
## FAN conn



## JIO S/B

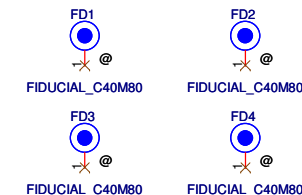
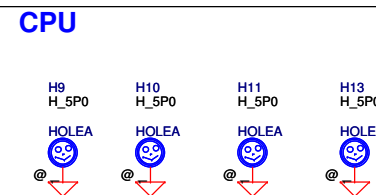
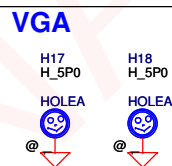
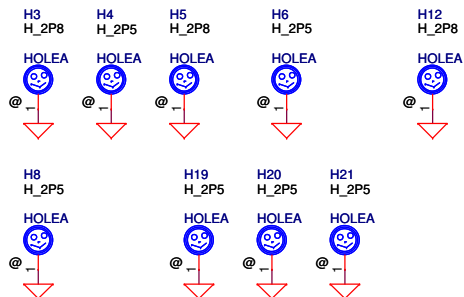
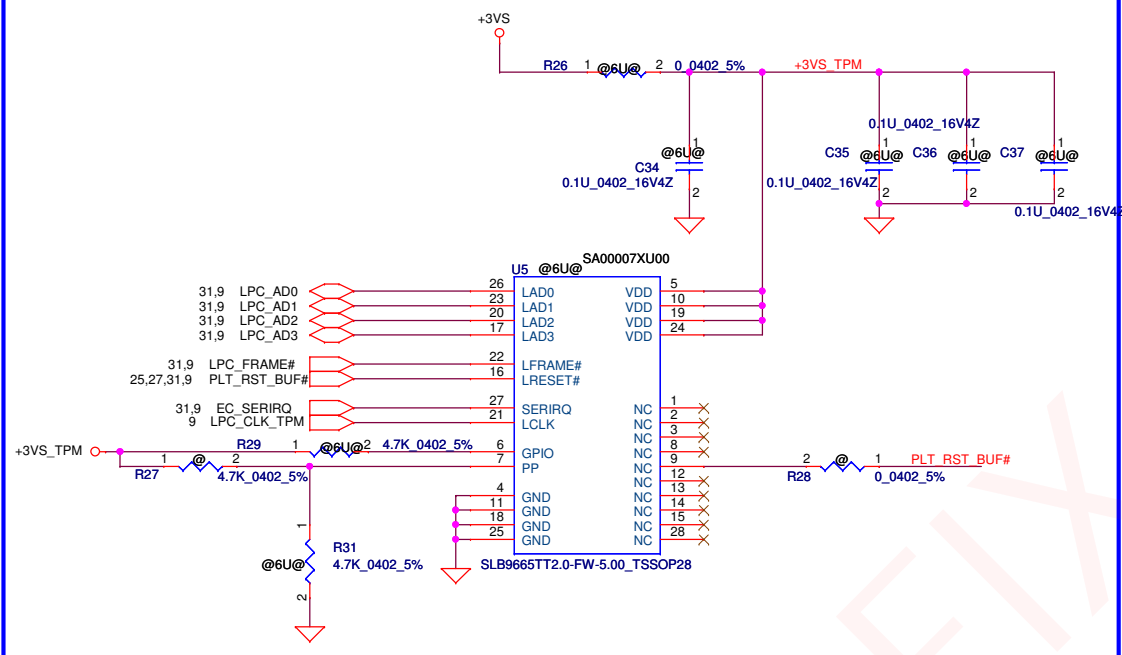


## CEM1,2 Close LM5/LM9



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	PWRBTN/FAN	
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					Document Number	
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# TPM2.0



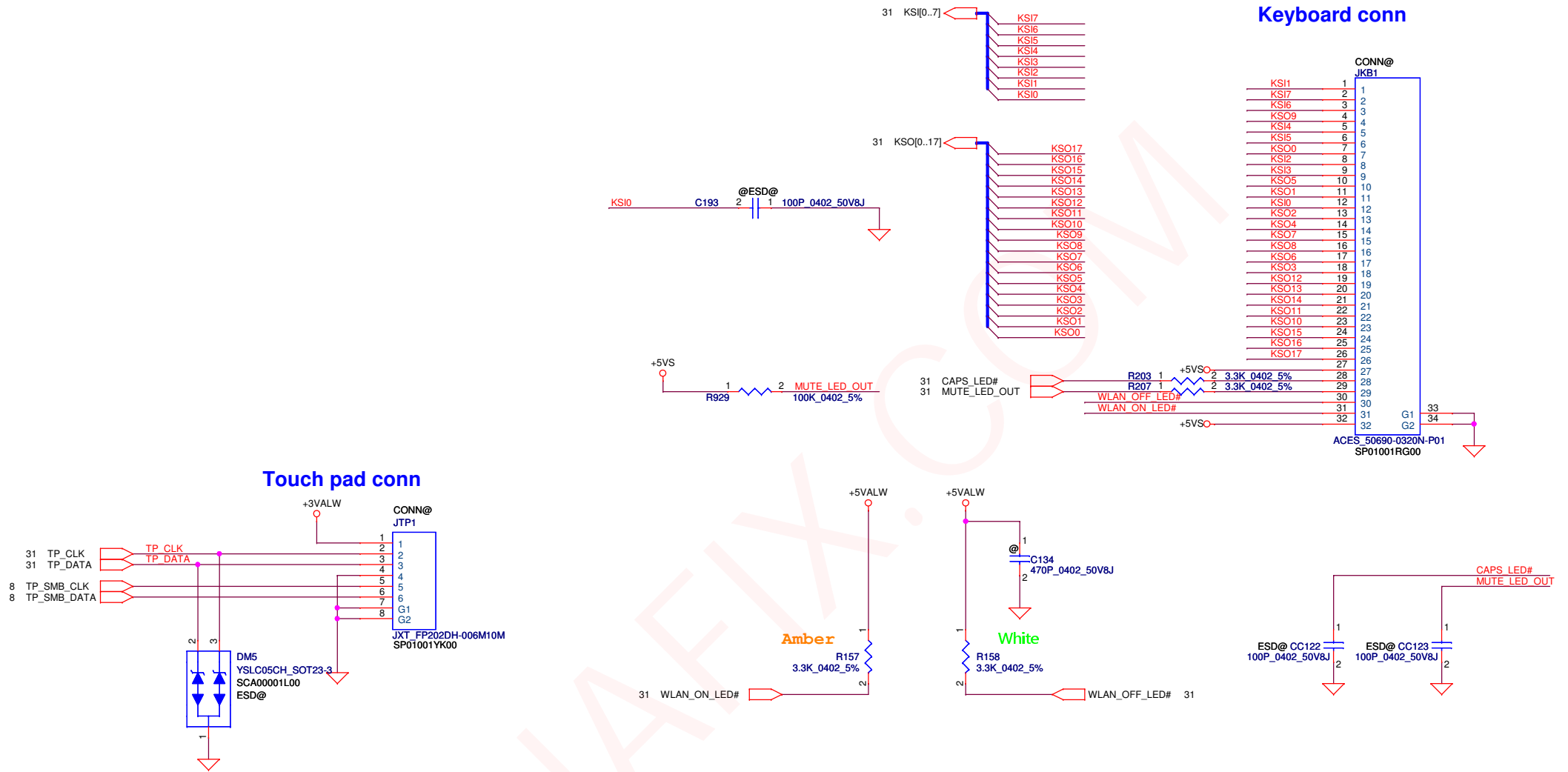
Security Classification	Compal Secret Data			Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	LED/Screw hole	
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				Document Number	0.1
				Date	Thursday, January 07, 2016
				Sheet	35 of 51

Compal Electronics, Inc.

LED/Screw hole

LA-706P

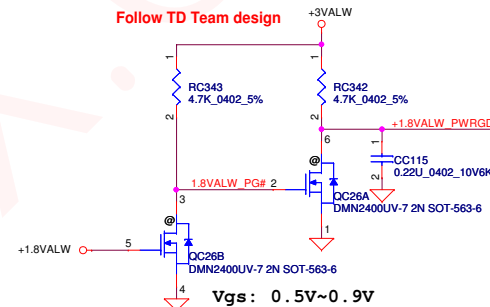
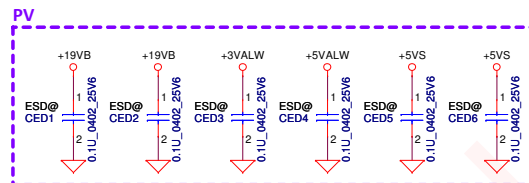
Thursday, January 07, 2016 Sheet 35 of 51



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP
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					LA-706P
				Date:	Thursday, January 07, 2016
				Sheet	36 of 51
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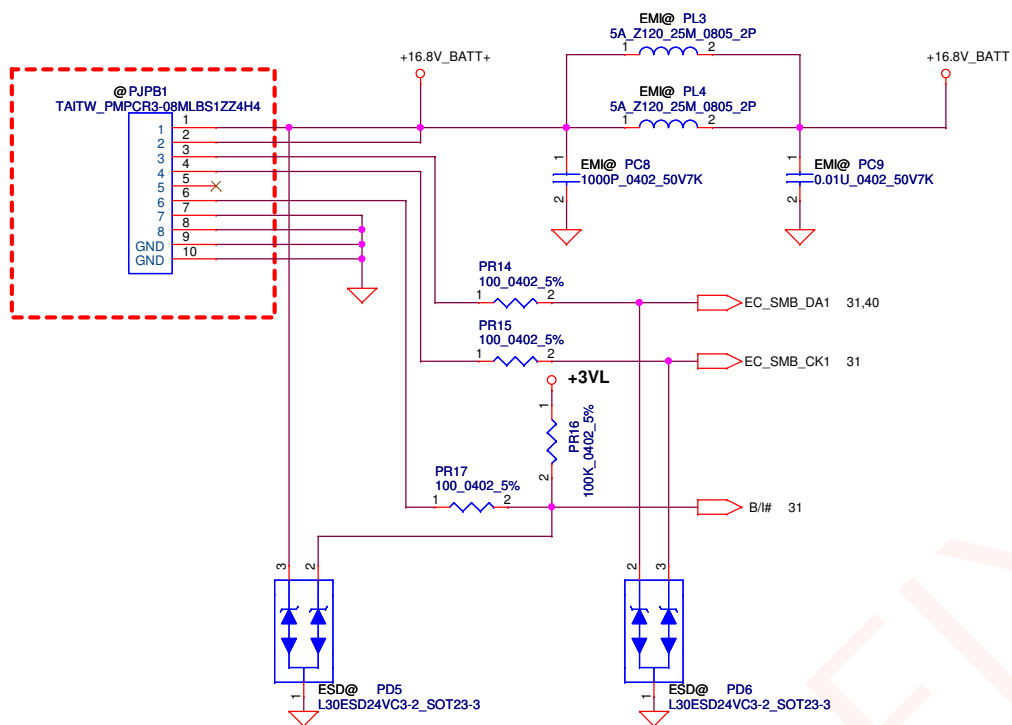


**SPOK** **2** **1** **+3V\_SOC\_ON**  
**R1061** **47K\_0402\_5%**



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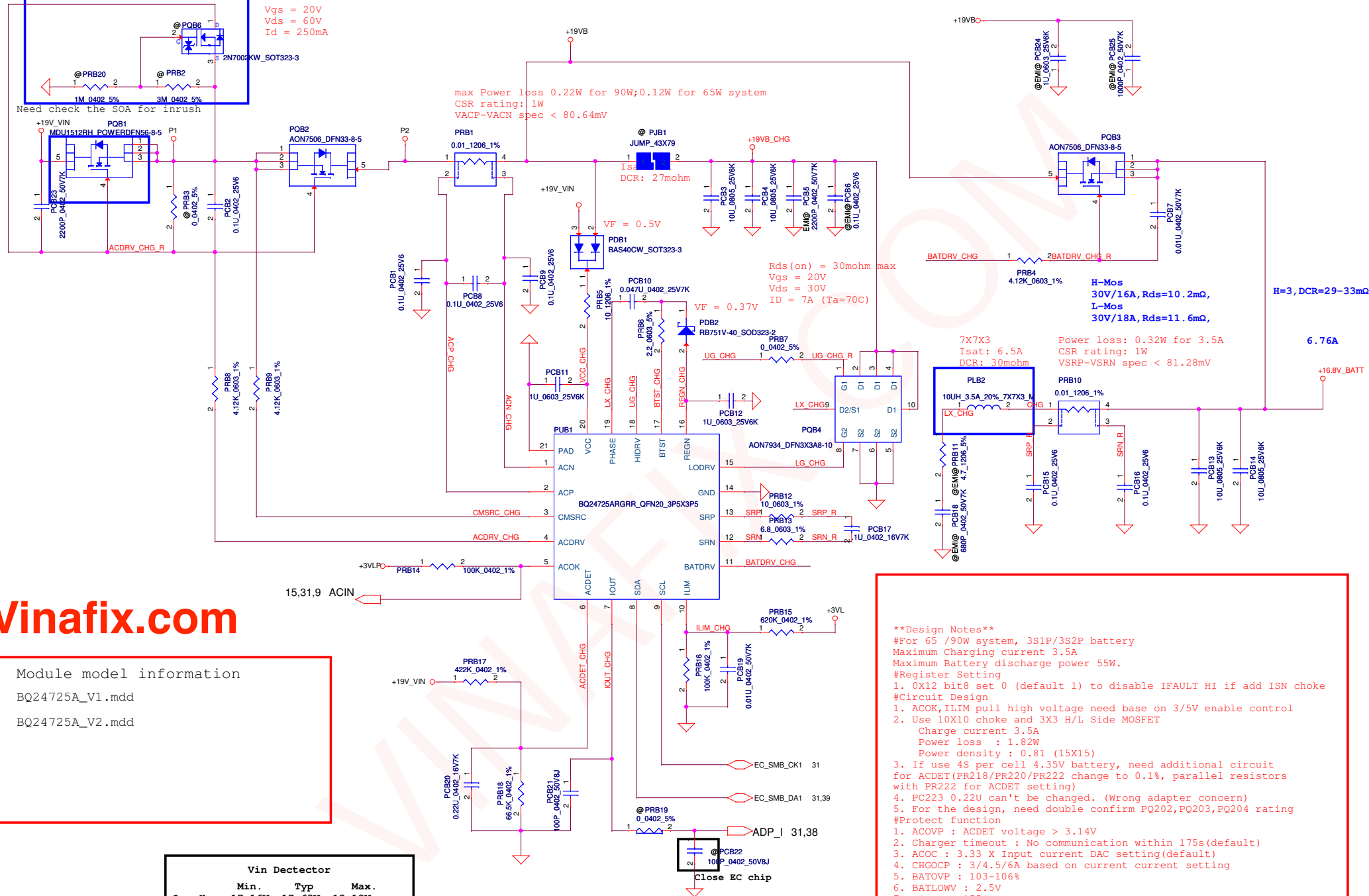
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/08	Deciphered Date	2016/08/06	Title	BATT Conn
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# Protection for reverse input

Vgs = 20V  
Vds = 60V  
Id = 250mA

Need check the SOA for inrush

max Power loss 0.22W for 90W;0.12W for 65W system  
CSR rating: 1W  
VACP-VACN spec < 80.64mV



# Vinafix.com

## Module model information

BQ24725A\_V1.mdd

BQ24725A\_V2.mdd

## Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20\*ILIM\*Rsr  
ILIM = 3.3\*100/(100+107)/20/0.02  
= 3.986 A

## \*\*Design Notes\*\*

#For 65 /90W system, 3S1P/3S2P battery  
Maximum Charging current 3.5A  
Maximum Battery discharge power 55W.

## #Register Setting

- 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
- Use 10X10 choke and 3X3 H/L Side MOSFET  
Charge current 3.5A  
Power loss : 1.82W  
Power density : 0.81 (15X15)

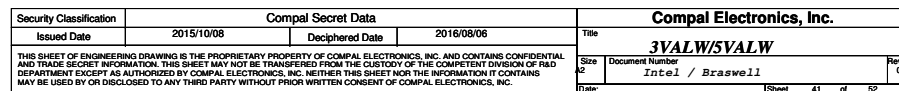
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)

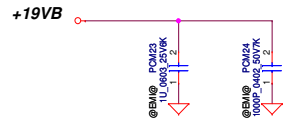
- PC223 0.22u can't be changed. (Wrong adapter concern)
- For the design, need double confirm PQ202,PQ203,PQ204 rating

## #Protect function

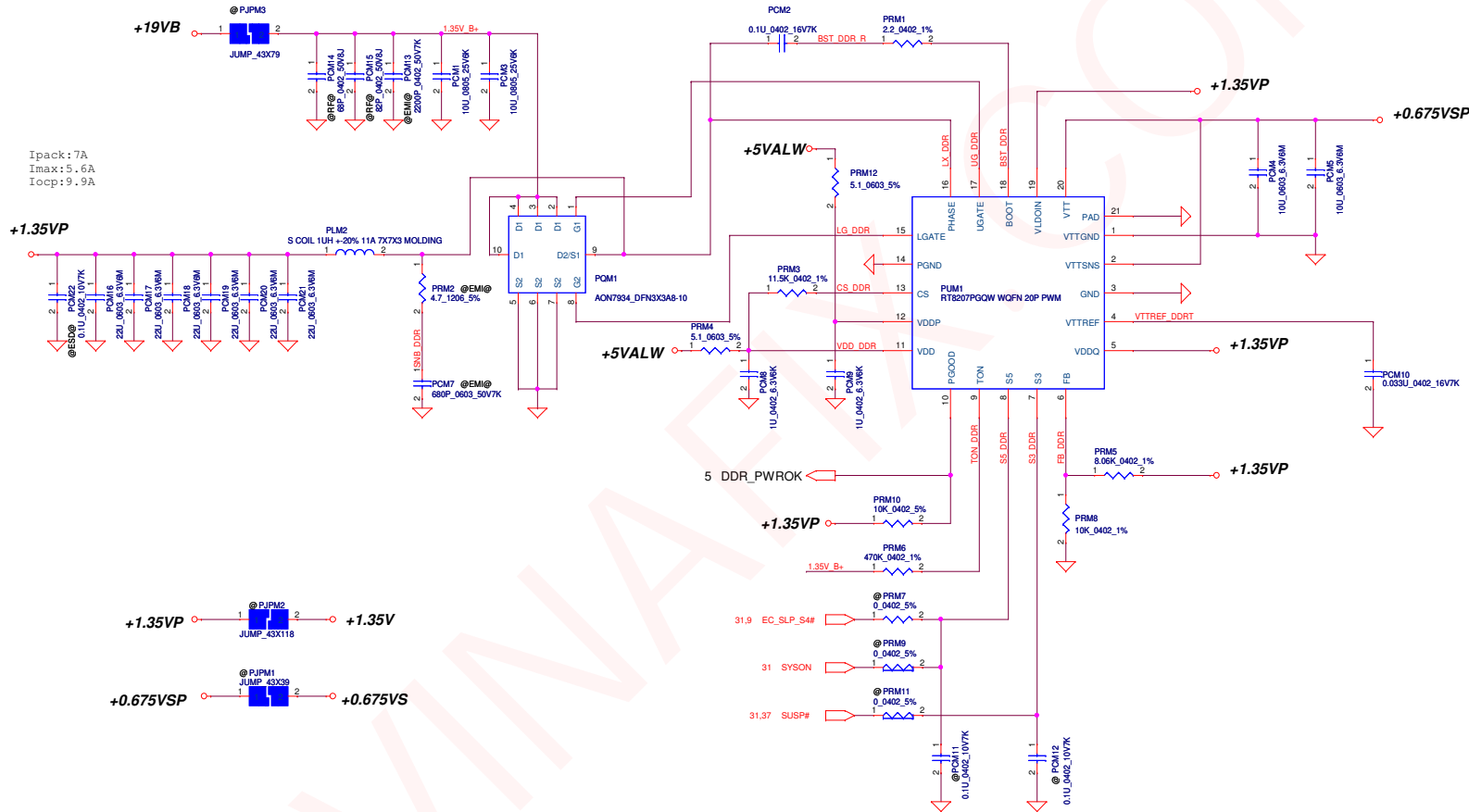
- ACOVF : ACDET voltage > 3.14V
- Charger timeout : No communication within 175s(default)
- ACOC : 3.33 X Input current DAC setting(default)
- CHGOCF : 3/4.5/6A based on current current setting
- BATOVP : 103-106%
- BATLOWV : 2.5V
- TSHUT : 155C
- IFAULT HI : 750mV (default)
- IFAULT LOW : 150mV (default)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/08	Deciphered Date	2012/07/02	CHARGER	
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				Intel / Braswell	Rev 0.1
				Date	Thursday, January 07, 2016
				Sheet	40 of 52



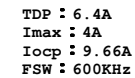


Ipack:7A  
Imax:5.6A  
Iocp:9.9A



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/08	Deciphered Date	2014/10/28	Title	1.35V/0.675VS
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				Date	Thursday, January 07, 2016
				Sheet	42 of 52
				Rev	0.1

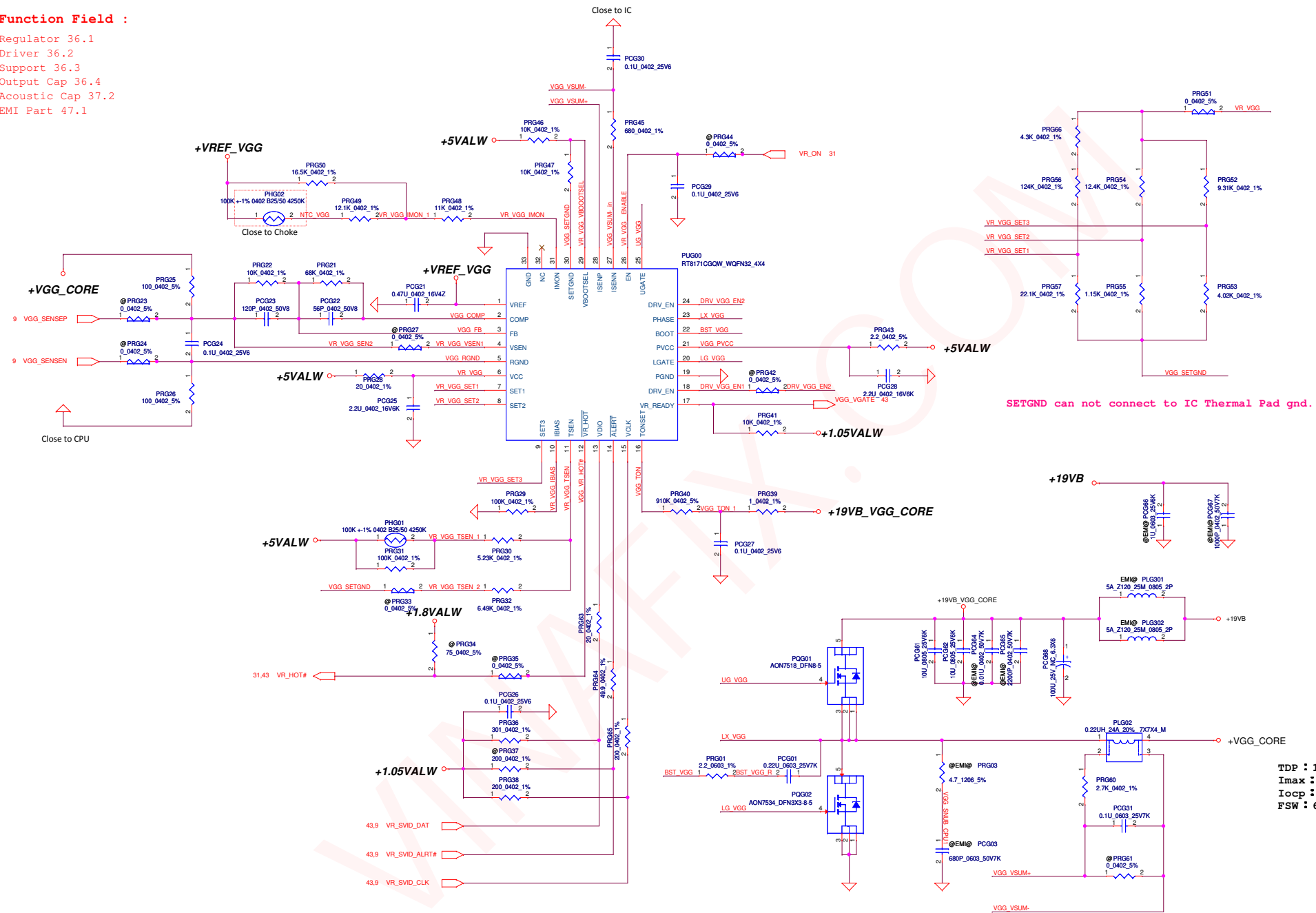
Regulator 36.1  
Driver 36.2  
Support 36.3  
Output Cap 36.4  
Acoustic Cap 37.2  
EMI Part 47.1



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Issued Date	2015/10/08	Deciphered Date	2013/07/10	Title <b>VCC_Core</b>		
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				Intel / Braswell		
Date:				Sheet	43	of 50

# Function Field :

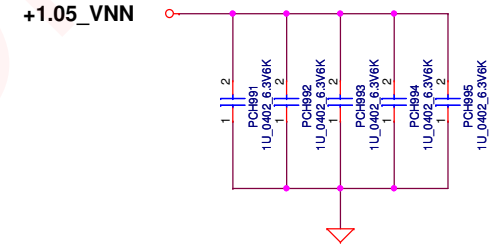
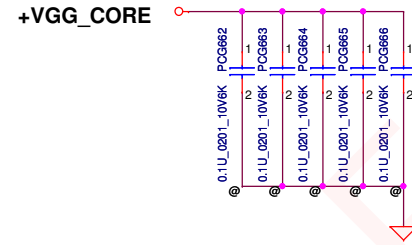
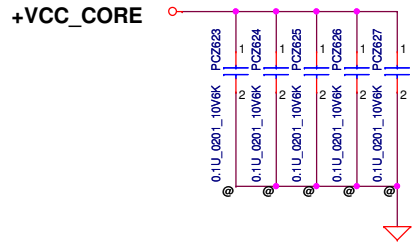
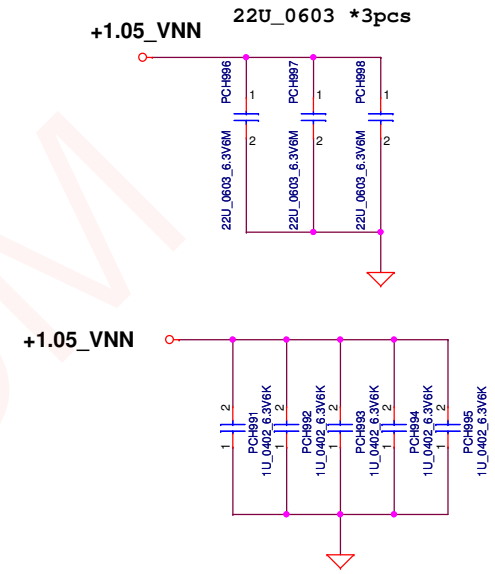
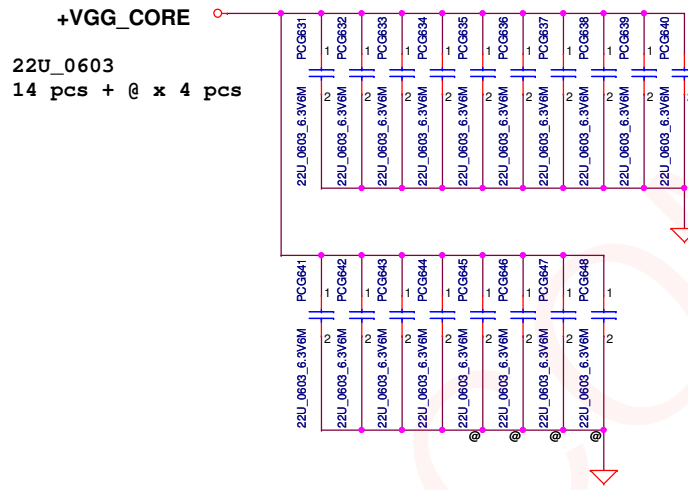
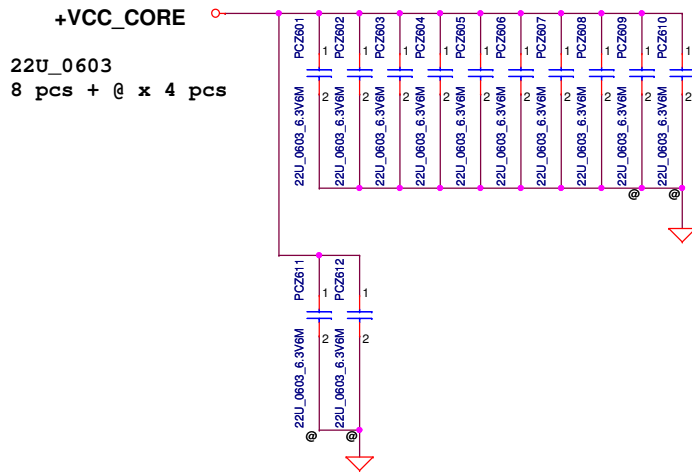
Regulator 36.1  
Driver 36.2  
Support 36.3  
Output Cap 36.4  
Acoustic Cap 37.2  
EMI Part 47.1



TDP : 11A  
Imax : 8.5A  
Iocp : 15.18A  
FSW : 600KHz

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Issued Date	2015/10/08	Deciphered Date	2013/07/10	Title	
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Size	C	Document Number	Intel / Braswell	Rev	0.1
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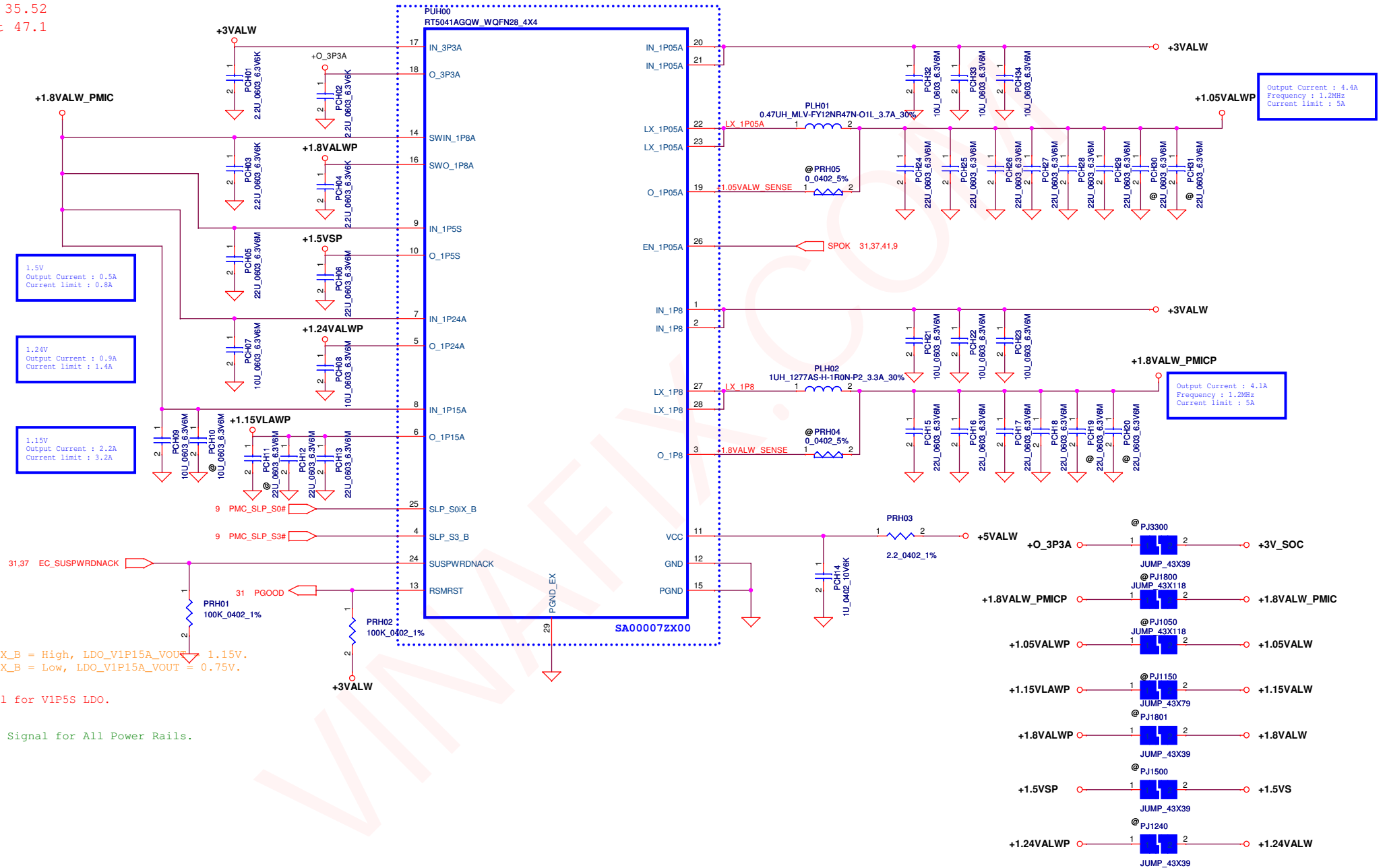
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/08	Deciphered Date	2015/07/08	Title	PWR-PROCESSOR DECOUPLING
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				Date: Thursday, January 07, 2016	Rev 0.1
				Sheet 45 of 52	

## Function Field :

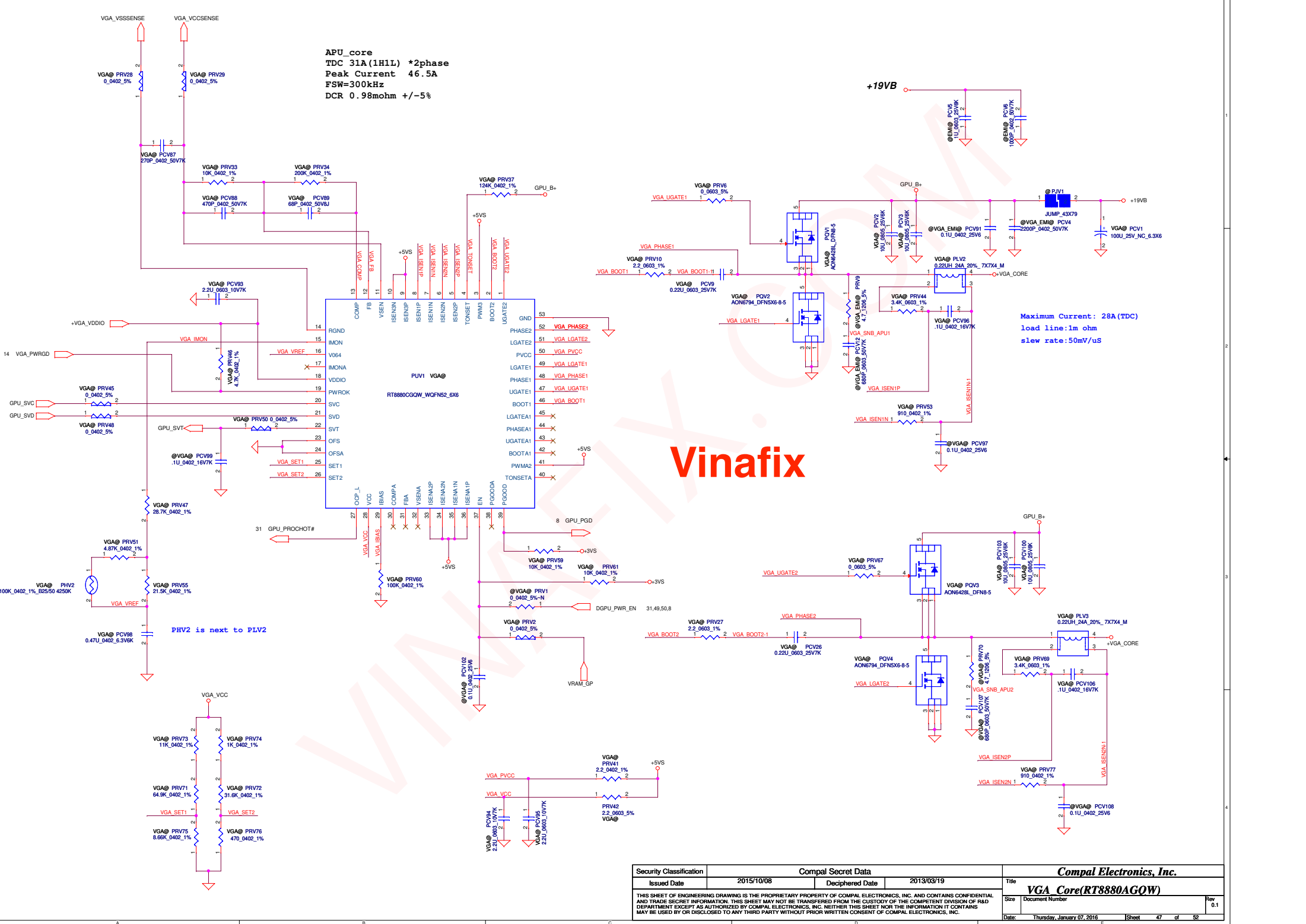
Regulator 35.51

Support 35.52

EMI Part 47.1



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				Date: Thursday, January 07, 2016	Rev 0.1
				Sheet 46	of 52



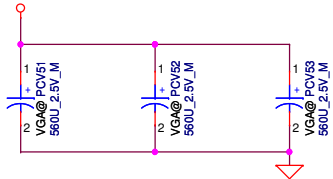
APU\_core  
TDC 31A(1H1L) \*2phase  
Peak Current 46.5A  
FSW=300kHz  
DCR 0.98mohm +/-5%

Maximum Current: 28A(TDC)  
load line:1m ohm  
slew rate:50mV/us

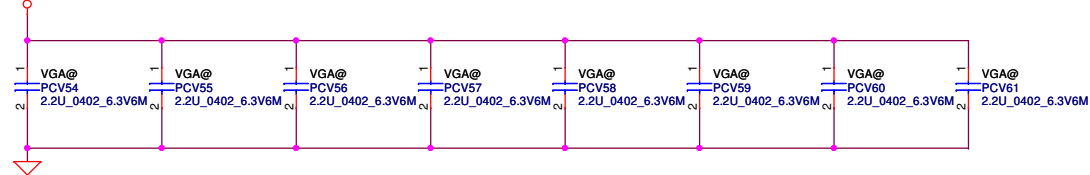
Vinafix

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Size	Document Number	Rev	0.1	
Date	Thursday, January 07, 2016	Sheet	47 of 52	

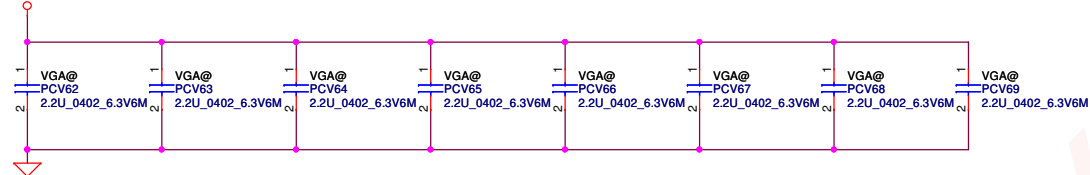
+VGA\_CORE



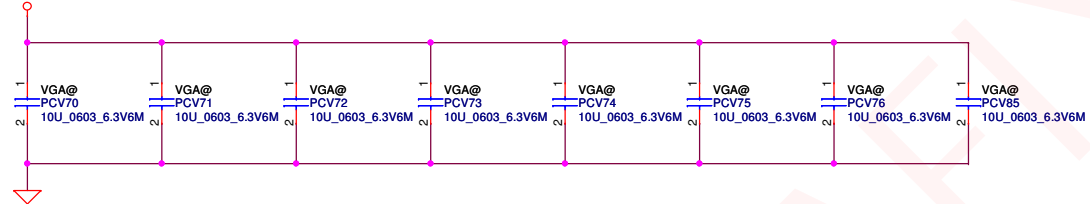
+VGA\_CORE



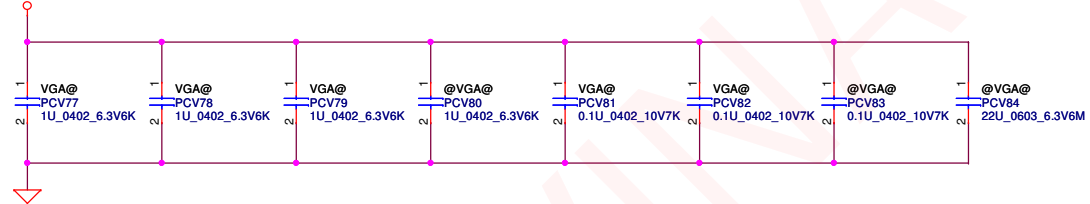
+VGA\_CORE



+VGA\_CORE



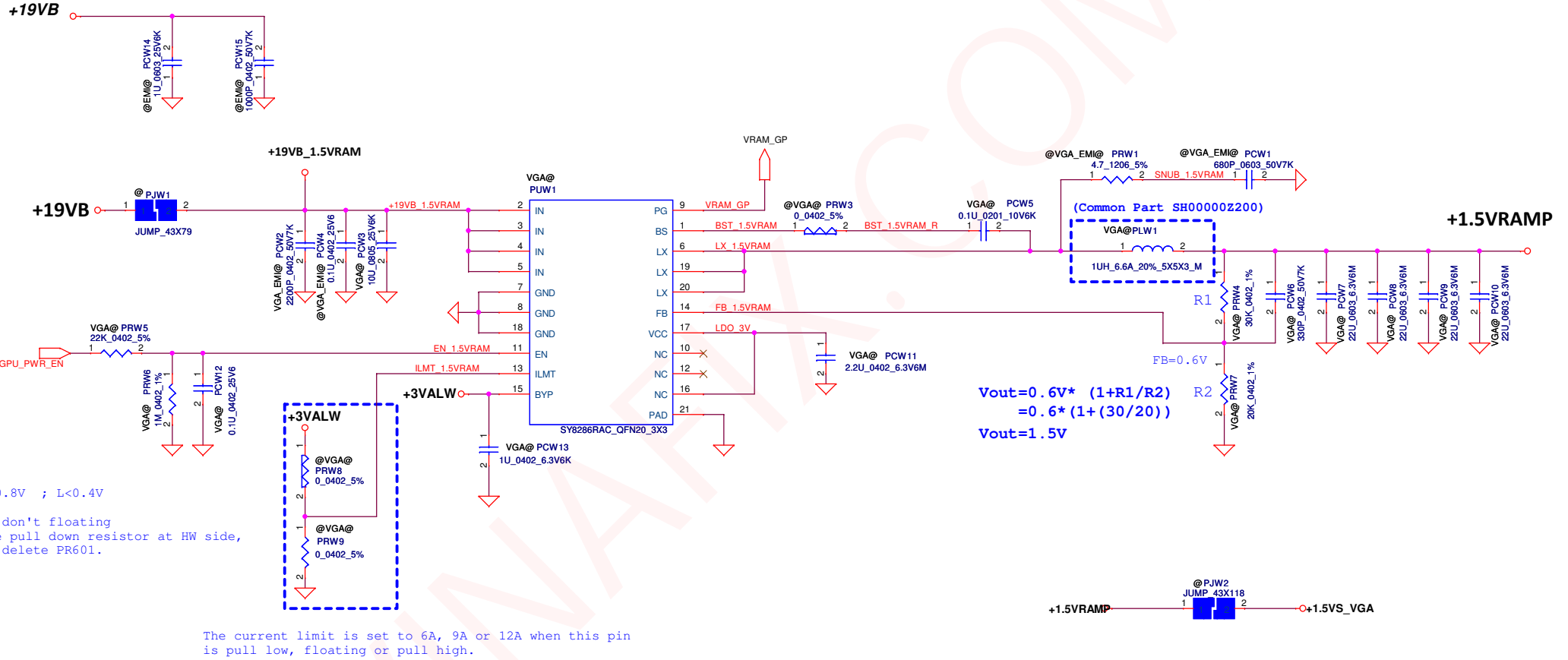
+VGA\_CORE



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Date:		Thursday, January 07, 2016		Sheet	48 of 52

## Module model information

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd



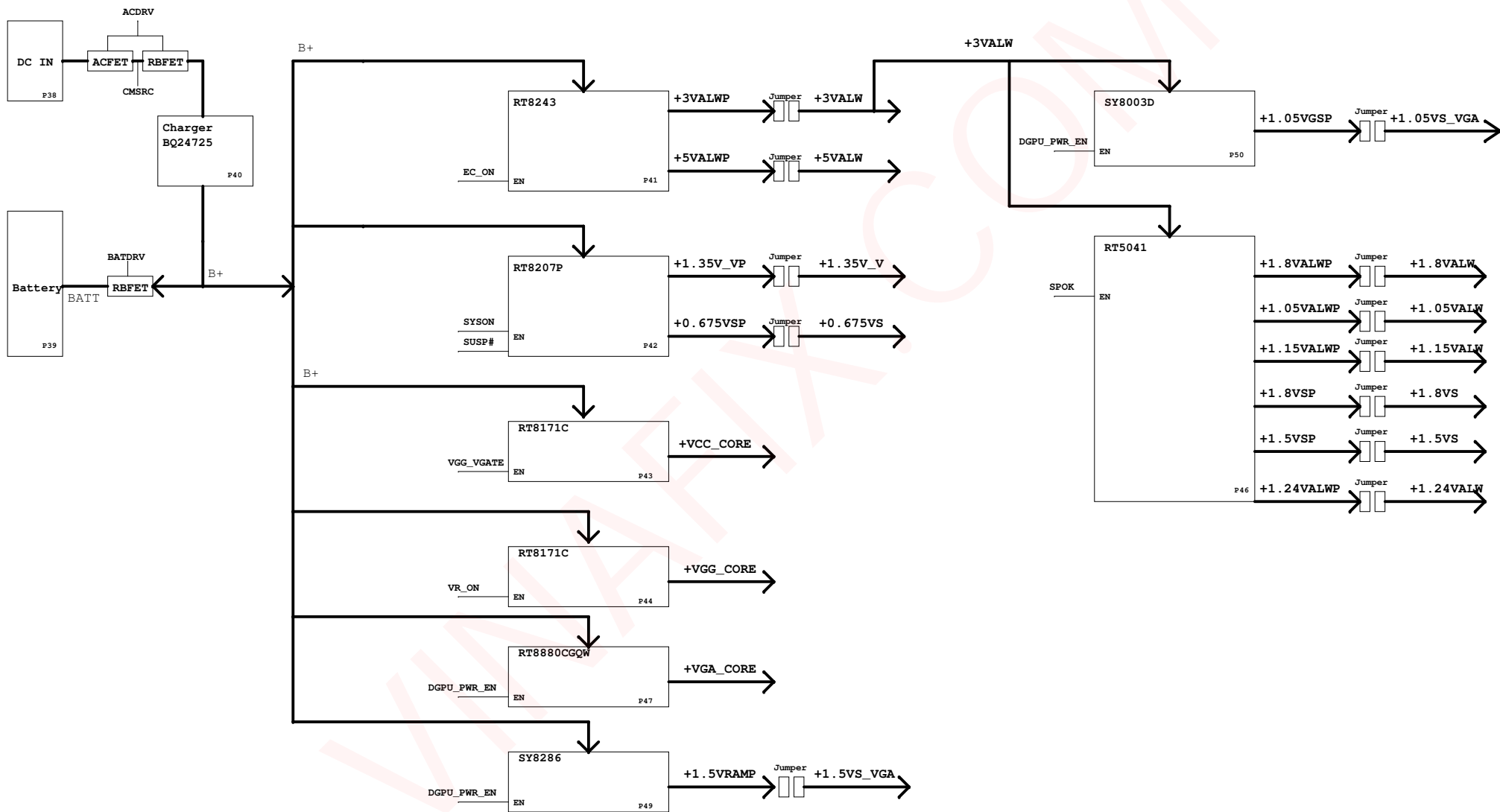
Security Classification	Compal Secret Data			APS55 Compal Electronics, Inc.		
Issued Date	2015/10/08	Deciphered Date	2014/05/26	Title	VRAM_1V5_GPU	
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## SY8003\_V2.mdd


$$V_{out} = 0.6V^* (1 + R_{up}/R_{down})$$

Note: Use VCCSA\_SEL to switch High & Low Level for VID[1] (ie. VCCSA\_SEL) due to the VID[0] is don't care for this setting.

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Issued Date	2015/10/08	Deciphered Date	2012/06/13	Title		
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				Size A3	Document Number	Rev 0.
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/08	Deciphered Date	2014/10/28	Title <b>Power Block Diagram</b>	
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Date: Thursday, January 07, 2016		Sheet 51 of 52			

Version change list (P.I.R. List)

Item	Date	Page	Reason for change	Modify List	Phase
1	11/16	P47	EE request for VGA power debug	Change PRV61 to stuff & PRV1/PCV102 to Unpop	SI
2	11/16	P47	EE request for VGA power debug	Add PRV2 for EE debug sequence issue	SI
3	11/24	P44	EMI request for debug	remove PJG1 & add PLG301/PLG302	SI
4	11/24	P52	EE request for VGA power debug	Change PRW5 0 ohm --> 22K & PCW12 0.1U to stuff	SI
5	11/24	P43	EMI request for debug	remove PJZ1 & add PLZ301/PLZ302	SI
6	12/29	P47	Modify OCP value	Change PRV73 1K-->11K, PRV71 124K-->64.9K PRV75 2.8K-->8.66K	PV
7	12/29	P40,P42	Diner cost down item	Change PCB17, PCM4 0603 to 0402, PCM5 0805 to 0603	PV
8	12/30	P43, P44, P47	Change 0 ohm to short pad	PRZ51, PRG51, PRV28, PRV29, PRV45, PRV48, PRV50, PRV2	PV
9	1/7	P49	Change 0 ohm to short pad	PRW8	PV
10					
11					
12					
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17					
18					
19					
20					
21					

Vinafix